

IT8720F

Environment Control – Low Pin Count Input / Output
(EC - LPC I/O)

Preliminary Specification V0.1

ITE TECH. INC.

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1. Features

■ Low Pin Count Interface

- Complies with Intel Low Pin Count Interface Specification Rev. 1.1
- Supports LDRQ#, SERIRQ protocols
- Supports PCI PME# Interfaces

■ ACPI & LANDesk Compliant

- ACPI V. 2.0 compliant
- Register sets compatible with "Plug and Play ISA Specification V. 1.0a"
- LANDesk 3.X compliant
- Supports 8 logical devices

■ Enhanced Hardware Monitor

- Built-in 8-bit Analog to Digital Converter
- 3 thermal inputs from either remote thermal resistor or thermal diode or diode-connected transistor, the temperature sensor of the current mode
- 7 voltage monitor inputs (VCCH and VBAT are measured internally.)
- 1 chassis open detection input with low power Flip-Flop dual-powered by battery or VCCH
- Watch Dog comparison of all monitored values
- Provides VID0 – VID7 support for the CPU
- Provides Serial-VID support for AMD CPU
- SST/PECI/AMDTSI I/F support

■ Fan Speed Controller

- Provides fan on-off and PWM control
- Supports 5 programmable Pulse Width Modulation (PWM) outputs
- 128 steps of PWM modes
- Monitors 5 fan tachometer inputs

■ SmartGuardian Controller

- Provides programmably automatic fan speed control
- Supports mix-and-match for temperature inputs and fan speed control outputs
- Overrides fan speed controller during catastrophic situations
- Provides audible over temperature warning

■ Two 16C550 UARTs

- Supports two standard Serial Ports
- Supports IrDA 1.0/ASKIR protocols

■ Consumer Remote Control (TV remote) IR with Power-up Feature

- Supports two CIR Ports

■ IEEE 1284 Parallel Port

- Standard mode -- Bi-directional SPP compliant
- Enhanced mode -- EPP V. 1.7 and V. 1.9 compliant
- High-speed mode -- ECP, IEEE 1284 compliant
- Back-drive current reduction
- Printer power-on damage reduction
- Supports POST (Power-On Self Test) Data Port

■ Floppy Disk Controller

- Supports two 360K/ 720K/ 1.2M/ 1.44M/ 2.88M floppy disk drives
- Enhanced digital data separator
- 3-Mode drives supported
- Supports automatic write protection via software

■ Keyboard Controller

- 8042 compatible with PS/2 keyboard and mouse
- Hardware KBC
- GateA20 and Keyboard reset output
- Supports Multiple keyboard power-on events (Any Key, 2-5 Sequential Keys, 1-3 simultaneous Keys)
- Supports mouse double-click and/or mouse move power on events

■ 63 General Purpose I/O Pins

- Input mode supports either switch de-bounce or programmable external IRQ input routing
- Output mode supports 2 sets of programmable LED blinking periods

■ Serial Flash I/F for BIOS

- Supports 32 M-bit of SPI I/F

■ Watch Dog Timer

- Time resolution 1 minute or 1 second, maximum 65535 minutes or 65535 seconds
- Output to KRST#, PCIRST# and PWROK when expired

■ ITE's Innovative Automatic Power-failure Resume and Power Button De-bounce

■ Dedicated Infrared Pins

■ AMD CPU Power Sequence Controller

- Built-in enhanced voltage comparator

- VCCH and Vbat Supported
- Built-in 32.768 KHz Oscillator
- Single 24/48 MHz Clock Input
- +5V Power Supply 128-pin QFP

2. General Description

The IT8720F is a highly integrated Super I/O using the Low Pin Count Interface. The IT8720F provides the most commonly used legacy Super I/O functionality plus the latest Environment Control initiatives, including H/W Monitor and Fan Speed Controller. The device's LPC interface complies with Intel "LPC Interface Specification Rev. 1.0". The IT8720F is ACPI & LANDesk compliant.

The IT8720F features the enhanced hardware monitor providing 3 thermal inputs from remote thermal resistors, or thermal diode or diode-connected transistor (2N3904/2N3906). The device employs ITE's innovative intelligent automatic Fan ON/OFF & speed control functions (SmartGuardian) to protect the system while reducing the system noise and power consumption.

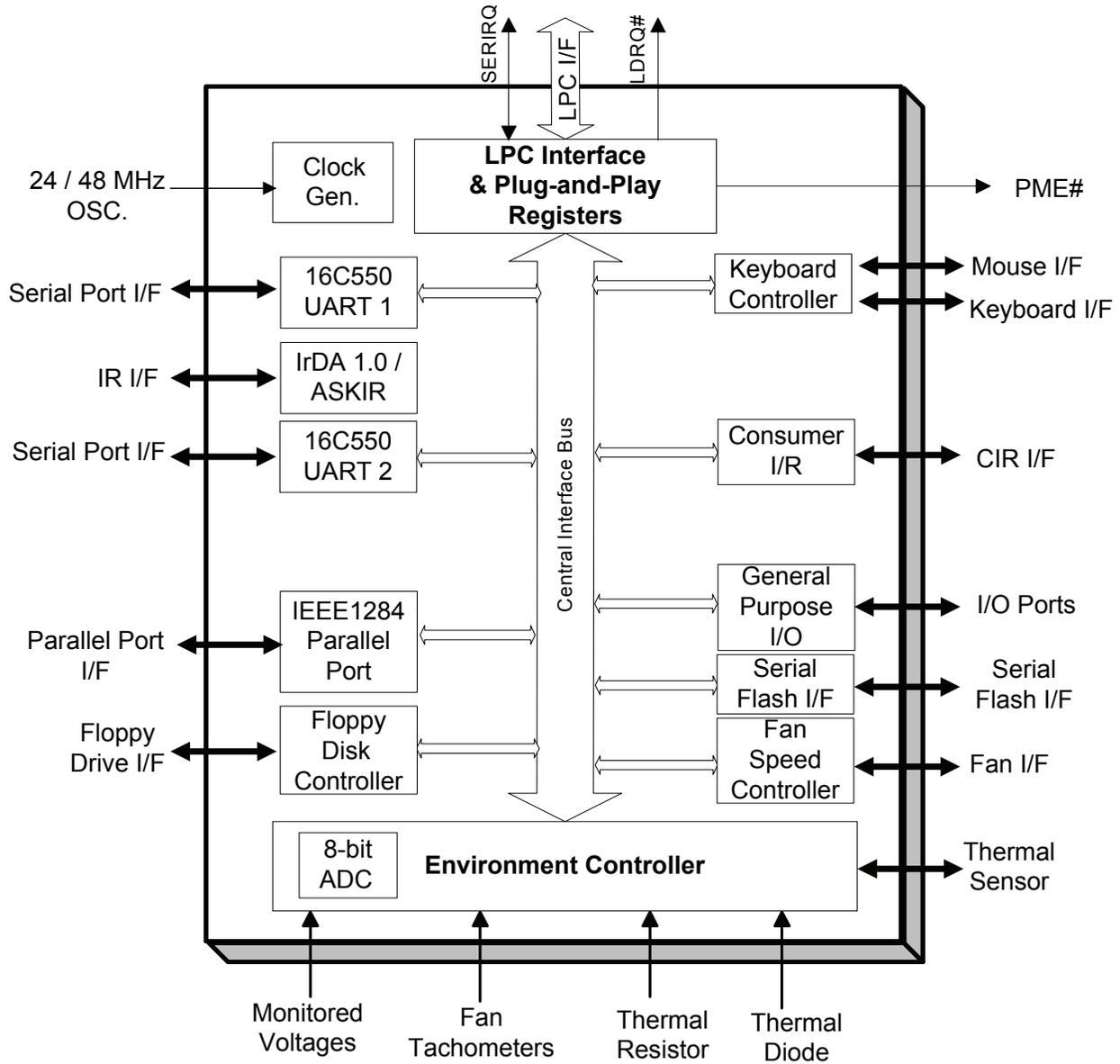
The IT8720F contains one Fan Speed Controller. The fan speed controller can control up to five fan speeds through three separate 128 steps of Pulse Width Modulation (PWM) output pins and monitor up to five FANs' Tachometer inputs. It also features two 16C550 UARTs, one IEEE 1284 Parallel Port, one Floppy Disk Controller and one Keyboard Controller.

Integrated in the IT8720F are eight logical devices. One high-performance 2.88MB floppy disk controller, with digital data separator, supporting two drives in 360K/720K/1.2M/1.44M/2.88M format. One multi-mode high-performance parallel port supporting bi-directional Standard Parallel Port (SPP), Enhanced Parallel Port (EPP V. 1.7 and EPP V. 1.9), and IEEE 1284 compliant Extended Capabilities Port (ECP). Two 16C550 standard compatible enhanced UARTs perform asynchronous communication, and also support IR interface. The device also features one fan speed controller which controls and monitors five fans, and eight GPIO ports controlling up to 63 GPIO pins. The IT8720F also has an integrated Keyboard Controller.

These eight logical devices can be individually enabled or disabled via software configuration registers. The IT8720F utilizes power-saving circuitry to reduce power consumption, and once a logical device is disabled, the inputs are inhibited with the clock disabled and the outputs are tri-stated. The device requires a single 24/48 MHz clock input and operates with +5V power supply. The IT8720F is available in 128-pin QFP (Quad Flat Package).

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3. Block Diagram



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4. Pin Configuration

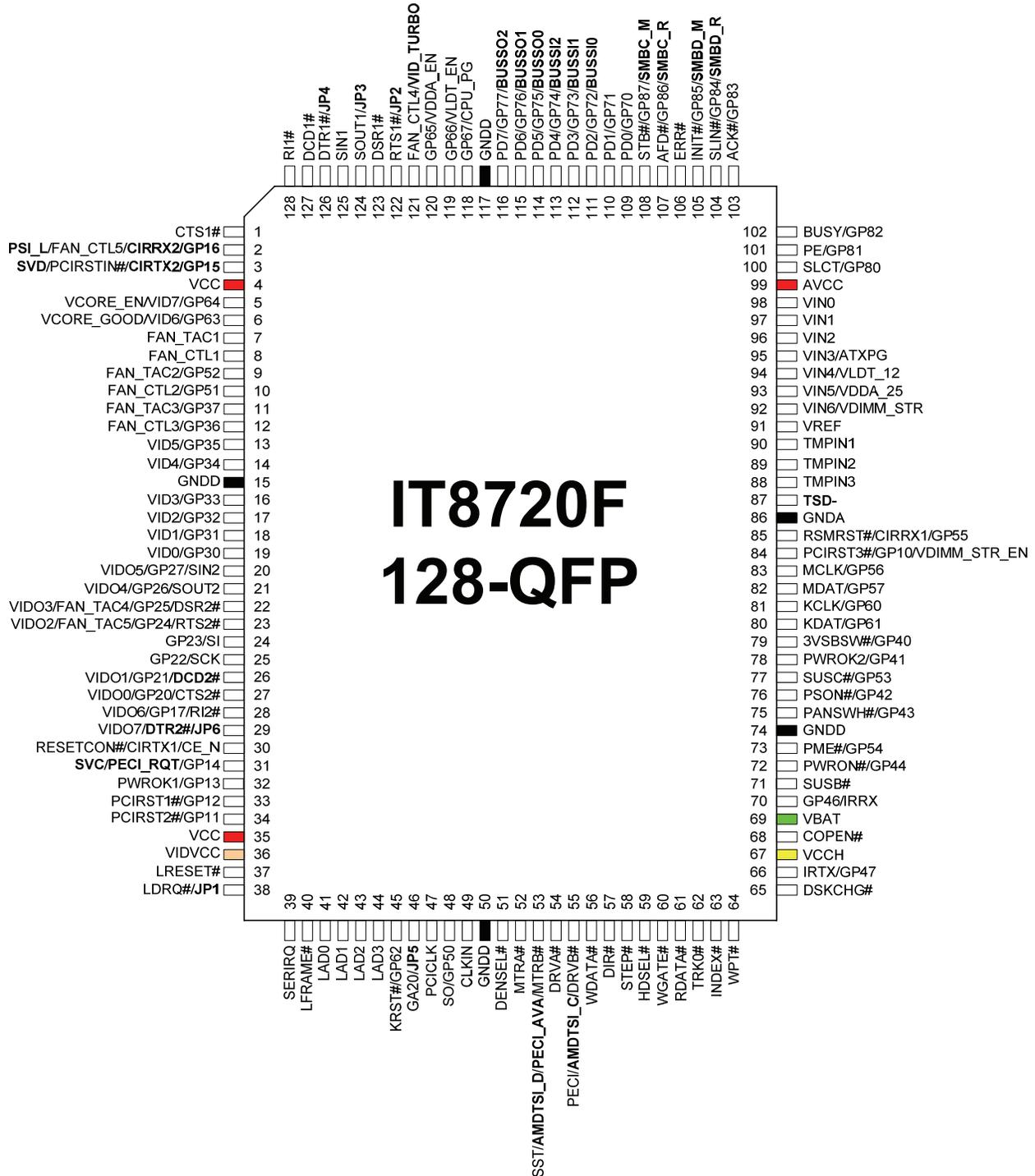


Figure 4-1. IT8720F 128-QFP

Note: The bold indicates the pin has changed since last revision.

Table 4-1. Pins Listed in Numeric Order

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	CTS1#	33	PCIRST1#/GP12	65	DSKCHG#	97	VIN1
2	PSI_L/FAN_CTL5/ CIRRX2/GP16	34	PCIRST2#/GP11	66	IRTX/GP47	98	VIN0
3	SVD/PCIRSTIN#/ CIRTX2/GP15	35	VCC	67	VCCH	99	AVCC
4	VCC	36	VIDVCC	68	COPEN#	100	SLCT/GP80
5	VCORE_EN/ VID7/GP64	37	LRESET#	69	VBAT	101	PE/GP81
6	VCORE_GOOD/ VID6/GP63	38	LDRQ#/JP1	70	GP46/IRRX	102	BUSY/GP82
7	FAN_TAC1	39	SERIRQ	71	SUSB#	103	ACK#/GP83
8	FAN_CTL1	40	LFRAME#	72	PWRON#/GP44	104	SLIN#/GP84/ SMBD_R
9	FAN_TAC2/GP52	41	LAD0	73	PME#/GP54	105	INIT#/GP85/ SMBD_M
10	FAN_CTL2/GP51	42	LAD1	74	GNDD	106	ERR#
11	FAN_TAC3/GP37	43	LAD2	75	PANSWH#/GP43	107	AFD#/GP86/ SMBC_R
12	FAN_CTL3/GP36	44	LAD3	76	PSON#/GP42	108	STB#/GP87/ SMBC_M
13	VID5/GP35	45	KRST#/GP62	77	SUSC#/GP53	109	PD0/GP70
14	VID4/GP34	46	GA20/JP5	78	PWROK2/GP41	110	PD1/GP71
15	GNDD	47	PCICLK	79	3VSBSW#/ GP40	111	PD2/GP72/ BUSS10
16	VID3/GP33	48	SO/GP50	80	KDAT/GP61	112	PD3/GP73/ BUSS11
17	VID2/GP32	49	CLKIN	81	KCLK/GP60	113	PD4/GP74/ BUSS12
18	VID1/GP31	50	GNDD	82	MDAT/GP57	114	PD5/GP75/ BUSS00
19	VID0/GP30	51	DENSEL#	83	MCLK/GP56	115	PD6/GP76/ BUSS01
20	VIDO5/GP27/SIN2	52	MTRA#	84	PCIRST3#/GP10/ VDIMM_STR_EN	116	PD7/GP77/ BUSUO2
21	VIDO4/GP26/ SOUT2	53	SST/AMDTSI_D/ PECI_AVA/MTRB#	85	RSMRST#/ CIRRX1/GP55	117	GNDD
22	VIDO3/FAN_TAC4/ GP25/DSR2#	54	DRVA#	86	GNDA	118	GP67/CPU_PG
23	VIDO2/FAN_TAC5/ GP24/RTS2#	55	PECI/AMDTSI_C/ DRVB#	87	TSD-	119	GP66/VLDT_EN
24	GP23/SI	56	WDATA#	88	TMPIN3	120	GP65/VDDA_EN
25	GP22/SCK	57	DIR#	89	TMPIN2	121	FAN_CTL4/ VID_TURBO
26	VIDO1/GP21/ DCD2#	58	STEP#	90	TMPIN1	122	RTS1#/JP2
27	VIDO0/GP20/ CTS2#	59	HDSEL#	91	VREF	123	DSR1#
28	VIDO6/GP17/RI2#	60	WGATE#	92	VIN6/VDIMM_STR	124	SOUT1/JP3
29	VIDO7/GP16/ DTR2#/JP6	61	RDATA#	93	VIN5/VDDA25	125	SIN1
30	RESETCON# /CIRTX1/CE_N	62	TRK0#	94	VIN4/VLDT_12	126	DTR1#/JP4
31	SVC/PECI_RQT/ GP14	63	INDEX#	95	VIN3/ATXPG	127	DCD1#
32	PWROK1/GP13	64	WPT#	96	VIN2	128	RI1#

5. IT8720F Pin Descriptions

Table 5-1. Pin Description of Supplies Signals

Pin(s) No.	Symbol	Attribute	Power	Description
4, 35	VCC	PWR	-	+5V Power Supply.
99	AVCC	PWR	-	+5V Analog Power Supply.
67	VCCH	PWR	-	+5V VCC Help Supply.
69	VBAT	PWR	-	+3.3V Battery Supply.
36	VIDVCC	PWR	-	VID power supply. (1.2 or 3.3V)
15, 50, 74, 117	GNDD	GND	-	Digital Ground.
86	GNDA	GND	-	Analog Ground.

Table 5-2. Pin Description of LPC Bus Interface Signals

Pin(s) No.	Symbol	Attribute	Power	Description
37	LRESET#	DI	VCC	LPC RESET #. EC block will not be reset by LRESET#, which is controlled by VCC PWRGD.
38	LDRQ#/JP1	DO16	VCC	LPC DMA Request #. This is an encoded signal for DMA channel select. During LRESET#, this pin is input for JP1 power-on strapping option.
39	SERIRQ	DIO16	VCC	Serial IRQ.
40	LFRAME#	DI	VCC	LPC Frame #. This signal indicates the start of the LPC cycle.
41-44	LAD[0:3]	DIO16	VCC	LPC Address / Data 0-3. 4-bit LPC address/bi-directional data lines. LAD0 is the LSB and LAD3 is the MSB.
47	PCICLK	DI	VCC	PCI Clock. 33 MHz PCI clock input for LPC I/F and SERIRQ.
73	PME#/GP54	DOD8/ DIOD8	VCCH	Power Management Event # / General Purpose I/O 54. <ul style="list-style-type: none"> The first function of this pin is the power management event #. It supports the PCI PME# interface. This signal allows the peripheral to request the system to wake up from the D3 (cold) state. The second function of this pin is the General Purpose I/O Port 5 Bit 4. The function configuration of this pin is determined by programming the software configuration registers.

Table 5-3. Pin Description of GPIO Signals

Pin(s) No.	Symbol	Attribute	Power	Description
48	SO/ GP50	DI/ DIOD8	VCC	Serial Flash Data Output / General Purpose I/O 50. <ul style="list-style-type: none"> The first function of this pin is Serial Data Output from Serial Flash. The second function of this pin is the General Purpose I/O Port 5 Bit 0. The function configuration of this pin is decided by the software configuration registers.
28	VIDO6/ GP17 / RI2#	DO8/ DIOD8/ DI	VCC	VIDO output 6 / General Purpose I/O 17 / Ring Indicator. <ul style="list-style-type: none"> The first function of this pin is VID output pin 6. The second function of this pin is the General Purpose I/O Port 1 Bit 7. The third function of this pin is Ring Indicator 2 #. See RI1# description. The function configuration of this pin is decided by the power-on strapping option (JP2) and software configuration registers.
29	VIDO7/ DTR2#/ CE_IN/ JP6	DO8/ DO8/ DI/ DI	VCC	VIDO output 7 / Data Terminal Ready 2 # / Chip Enable Input. <ul style="list-style-type: none"> The first function of this pin is VID output pin 7. The second function of this pin is Data Terminal Ready 2 #. See DTR1# description. The third function of this pin is Chip Enable Input and it is for GA only. The function configuration of this pin is decided by the power-on strapping option (JP2) and software configuration registers. During LRESET#, this pin is input for JP6 power-on strapping option.
27	VIDO0/ GP20/ CTS2#	DO8/ DIOD8/ DO8	VCC	VID output 0 / General Purpose I/O 20 / Clear to Send 2 #. <ul style="list-style-type: none"> The first function of this pin is VID output pin 0. The second function of this pin is the General Purpose I/O Port 2 Bit 0. The third function of this pin is Clear to Send 2 #. See CTS1# description. The function configuration of this pin is decided by the power-on strapping option (JP2) and software configuration registers.
26	VIDO1/ GP21/ DCD2#	DO8/ DIOD8/ DI	VCC	VID output 1 / General Purpose I/O 21 / Data Carrier Detect 2 #. <ul style="list-style-type: none"> The first function of this pin is VID output pin 1. The second function of this pin is the General Purpose I/O Port 2 Bit 1. The third function of this pin is Data Carrier Detect 2 #. See RI1# description. The function configuration of this pin is decided by the power-on strapping option (JP2) and software configuration registers.
25	GP22/ SCK	DIOD8/ DOD8	VCC	General Purpose I/O 22 / Serial Flash Clock. <ul style="list-style-type: none"> The first function of this pin is the General Purpose I/O Port 2 Bit 2. The second function of this pin is Serial Clock for Serial Flash. Note: Place the SPI device as close to IT8720 as possible. The function configuration of this pin is determined by programming the software configuration registers.

Pin(s) No.	Symbol	Attribute	Power	Description
24	GP23/ SI	DIOD8/ DOD8	VCC	General Purpose I/O 23 / Serial Flash In Data. <ul style="list-style-type: none"> The first function of this pin is the General Purpose I/O Port 2 Bit 3. The second function is Serial In Data for Serial Flash. The function configuration of this pin is determined by programming the software configuration registers.
23	VIDO2/ FAN_TAC5/ GP24/ RTS2#	DO8/ DI/ DIOD8/ DO8	VCC	VID output 2 / FAN Tachometer input 5/ General Purpose I/O 24 / Request to Send 2 #. <ul style="list-style-type: none"> The first function of this pin is VID output pin 2. The second function of this pin is Fan Tachometer Input 5. 0 to +5V amplitude fan tachometer input. The third function of this pin is the General Purpose I/O Port 2 Bit 4. The fourth function of this pin is Request to Send 2 #. See RTS1# description. The function configuration of this pin is decided by the power-on strapping option (JP2) and software configuration registers.
22	VIDO3/ FAN_TAC4/ GP25/ DSR2#	DO8/ DI/ DIOD8/ DI	VCC	VID output 3 / FAN Tachometer input 5 / General Purpose I/O 25 / Data Set Ready 2 #. <ul style="list-style-type: none"> The first function of this pin is VID output pin 3. The second function of this pin is Fan Tachometer Input 4. 0 to +5V amplitude fan tachometer input. The third function of this pin is the General Purpose I/O Port 2 Bit 5. The fourth function of this pin is Data Set Ready 2 #. See DSR1# description. The function configuration of this pin is decided by the power-on strapping option (JP2) and software configuration registers.
21	VIDO4/ GP26/ SOUT2	DO8/ DIOD8 /DO8	VCC	VID output 4 / General Purpose I/O 26 / Serial Data Output 2. <ul style="list-style-type: none"> The first function of this pin is VID output pin 4. The second function of this pin is the General Purpose I/O Port 2 Bit 6. The third function of this pin is Serial Data Output 2. See SOUT1 description. The function configuration of this pin is decided by the power-on strapping option (JP2) and software configuration registers.
20	VIDO5/ GP27/ SIN2	DO8/ DOD8/ DI	VCC	VID output 5 / General Purpose I/O 27 / Serial Data Input 2. <ul style="list-style-type: none"> The first function of this pin is VID output pin 5. The second function of this pin is the General Purpose I/O Port 2 Bit 7. The third function of this pin is Serial Data Input 2. See SIN1 description. The function configuration of this pin is decided by the power-on strapping option (JP2) and software configuration registers.
118	GP67/ CPU_PG	DIOD8/ DOD8	VCC	General Purpose I/O 67 / CPU Power-good <ul style="list-style-type: none"> The first function of this pin is the General Purpose I/O Port 6 Bit 7. The second function of this output pin is to indicate that CPU power-good is ready. The external pull high resistor is required. The function configuration of this pin is decided by the power-on strapping option (JP4) and software configuration registers.

Pin(s) No.	Symbol	Attribute	Power	Description
119	GP66/ VLDT_EN	DIOD8/ DOD8	VCC	<p>General Purpose I/O 66 / VLDT Enable</p> <ul style="list-style-type: none"> The first function of this pin is the General Purpose I/O Port 6 Bit 6. The second function of this pin is to enable VLDT Voltage. The external pull high resistor is required. <p>The function configuration of this pin is decided by the power-on strapping option (JP4) and software configuration registers.</p>
120	GP65/ VDDA_EN	DIOD8/ DOD8	VCC	<p>General Purpose I/O 65 / VDDA Enable</p> <ul style="list-style-type: none"> The first function of this pin is the General Purpose I/O Port 6 Bit 5. The second function of this pin is to enable VDDA power. The external pull high resistor is required. <p>The function configuration of this pin is decided by the power-on strapping option (JP4) and software configuration registers.</p>

Table 5-4. Pin Description of Hardware Monitor Signals^{Note1}

Pin(s) No.	Symbol	Attribute	Power	Description
98, 97, 96	VIN[0:2]	AI	AVCC	Voltage Analog Inputs [0:2]. 0 to 4.096V FSR Analog Inputs.
95	ATXPG/ VIN3	DI/ AI	AVCC	Voltage Analog Input 3 / ATX Power Good. <ul style="list-style-type: none"> The first function of this pin is ATX Power Good. PWROK1/2 will be (<u>VCC power-level-detect AND RESETCON# AND SUSB# AND ATXPG</u>) if bit0 of Index 2Ch is 1, or (<u>VCC power-level-detect AND RESETCON# AND SUSB#</u>) if the bit is 0. The second function of this pin is 0 to 4.096V FSR Analog Inputs. The function configuration of this pin is determined by programming the software configuration registers.
94	VLDT_12/ VIN4	AI/ AI	AVCC	VLDT (1.2V) analog inputs / Voltage Analog Input 4. <ul style="list-style-type: none"> The first function of this pin is VLDT (1.2V) analog inputs. The second function of this pin is 0 to 4.096V FSR Analog Inputs. The function configuration of this pin is decided by the power-on strapping option (JP4) and software configuration registers.
93	VDDA_25/ VIN5	AI/AI	AVCC	VDDA (2.5V) analog inputs / Voltage Analog Input 5. <ul style="list-style-type: none"> The first function of this pin is VDDA (2.5V) analog inputs. The second function of this pin is 0 to 4.096V FSR Analog Inputs. The function configuration of this pin is decided by the power-on strapping option (JP4) and software configuration registers.
92	VDIMM_STR/ VIN6	AI/ AI	AVCC	VDIMM DUAL STR (1.8V) analog inputs / Voltage Analog Input 6. <ul style="list-style-type: none"> The first function of this pin is VDIMM DUAL STR (1.8V) analog inputs. The second function of this pin is 0 to 4.096V FSR Analog Inputs. The function configuration of this pin is decided by the power-on strapping option (JP4) and software configuration registers.
91	VREF	AO	AVCC	Reference Voltage Output. Regulated and referred voltage for external temperature sensors and negative voltage monitors.
88-90	TMPIN[1:3]	AI	AVCC	External Thermal Inputs [1:3]. Connected to thermistors [1:3] or thermal temperature sensors.
87	TS_D-	AI	AVCC	Thermal Diode Negative Input.
7	FAN_TAC1	DI	VCC	Fan Tachometer Input 1. 0 to +5V amplitude fan tachometer input.
9	FAN_TAC2/ GP52	DI/ DIOD8	VCC	Fan Tachometer Input 2 / General Purpose I/O 52. <ul style="list-style-type: none"> The first function of this pin is Fan Tachometer Input 2. 0 to +5V amplitude fan tachometer input. The second function of this pin is the General Purpose I/O Port 5 Bit 2. The function configuration of this pin is determined by programming the software configuration registers.
11	FAN_TAC3/ GP37	DI/ DIOD8	VCC	Fan Tachometer Input 3 / General Purpose I/O 37. <ul style="list-style-type: none"> The first function of this pin is Fan Tachometer Input 3. 0 to +5V amplitude fan tachometer input. The second function of this pin is the General Purpose I/O Port 5 Bit 2. The function configuration of this pin is determined by programming the software configuration registers.

Pin(s) No.	Symbol	Attribute	Power	Description
19	VID0/ GP30	DIO8/ DIOD8	VCC	<p>Voltage ID 0 / General Purpose I/O 30.</p> <ul style="list-style-type: none"> The first function of this pin is Voltage ID Input 0. The Voltage ID is the voltage supply readout from the CPU. This value is read from the VID register. (The input threshold is 0.8/0.4V.) The second function of this pin is the General Purpose I/O Port 3 Bit 0. <p>The function configuration of this pin is decided by the software configuration registers.</p>
18	VID1/ GP31	DIO8/ DIOD8	VCC	<p>Voltage ID 1 / General Purpose I/O 31.</p> <ul style="list-style-type: none"> The first function of this pin is Voltage ID Input 1. The Voltage ID is the voltage supply readout from the CPU. This value is read from the VID register. (The input threshold is 0.8/0.4V.) The second function of this pin is the General Purpose I/O Port 3 Bit 1. <p>The function configuration of this pin is decided by the software configuration registers.</p>
17	VID2/ GP32	DIO8/ DIOD8	VCC	<p>Voltage ID 2 / General Purpose I/O 32.</p> <ul style="list-style-type: none"> The first function of this pin is Voltage ID Input 2. The Voltage ID is the voltage supply readouts from the CPU. This value is read from the VID register. (The input threshold is 0.8/0.4V.) The second function of this pin is the General Purpose I/O Port 3 Bit 2. <p>The function configuration of this pin is decided by the software configuration registers.</p>
16	VID3/ GP33	DIO8/ DIOD8	VCC	<p>Voltage ID 3 / General Purpose I/O 33.</p> <ul style="list-style-type: none"> The first function of this pin is Voltage ID Input 3. The Voltage ID is the voltage supply readout from the CPU. This value is read from the VID register. (The input threshold is 0.8/0.4V.) The second function of this pin is the General Purpose I/O Port 3 Bit 3. <p>The function configuration of this pin is decided by the software configuration registers.</p>
14	VID4/ GP34	DIO8/ DIOD8	VCC	<p>Voltage ID 4 / General Purpose I/O 34.</p> <ul style="list-style-type: none"> The first function of this pin is Voltage ID Input 4. The Voltage ID is the voltage supply readout from the CPU. This value is read from the VID register. (The input threshold is 0.8/0.4V.) The second function of this pin is the General Purpose I/O Port 3 Bit 4. <p>The function configuration of this pin is decided by the software configuration registers.</p>
13	VID5/ GP35	DIO8/ DIOD8	VCC	<p>Voltage ID 5 / General Purpose I/O 35.</p> <ul style="list-style-type: none"> The first function of this pin is Voltage ID Input 5. The Voltage ID is the voltage supply readout from the CPU. This value is read from the VID register. (The input threshold is 0.8/0.4V.) The second function of this pin is the General Purpose I/O Port 3 Bit 5. <p>The function configuration of this pin is decided by the software configuration registers.</p>

Pin(s) No.	Symbol	Attribute	Power	Description
6	VID6/ GP63/ VCORE_GD	DIO8/ DIOD8/ DI	VCC	Voltage ID 6 / General Purpose I/O 63 / VCORE Power Good. <ul style="list-style-type: none"> The first function of this pin is Voltage ID Input 6. The Voltage ID is the voltage supply readout from the CPU. This value is read from the VID register. (The input threshold is 0.8/0.4V.) The second function of this pin is the General Purpose I/O Port 6 Bit 3. The third function of this pin is to indicate the power-good signal of CPU core voltage. The function configuration of this pin is decided by the software configuration registers.
5	VID7/ GP64/ VCORE_EN	DIO8/ DIOD8/ DOD8	VCC	Voltage ID 7 / General Purpose I/O 64 / VCORE Enable. <ul style="list-style-type: none"> The first function of this pin is Voltage ID Input 7. The Voltage ID is the voltage supply readout from the CPU. This value is read from the VID register. (The input threshold is 0.8/0.4V) The second function of this pin is the General Purpose I/O Port 6 Bit 4. The third function of this pin is VCORE Enable, which is to enable the PWM controller for CPU core voltage. The external pull high resistor is required. The function configuration of this pin is decided by the software configuration registers.
68	COPEN#	DIOD8	VCCH or VBAT	Case Open Detection #. <ul style="list-style-type: none"> The Case Open Detection is connected to a specially designed low power CMOS flip-flop dual-powered by battery or VCCH for case open state preservation during power loss.

Table 5-5. Pin Description of Fan Controller Signals

Pin(s) No.	Symbol	Attribute	Power	Description
8	FAN_CTL1	DOD8	VCC	Fan Control Output 1. (PWM output signal to Fan's FET.)
10	FAN_CTL2/ GP51	DOD8/ DIOD8	VCC	Fan Control Output 2 / General Purpose I/O 51. <ul style="list-style-type: none"> The first function of this pin is Fan Control Output 2. (PWM output signal to Fan's FET.) The second function of this pin is the General Purpose I/O Port 5 Bit 1. The function configuration of this pin is determined by programming the software configuration registers.
12	FAN_CTL3/ GP36	DOD8/ DIOD8	VCC	Fan Control Output 3 / General Purpose I/O 36. <ul style="list-style-type: none"> The first function of this pin is Fan Control Output 3. (PWM output signal to Fan's FET.) The second function of this pin is the General Purpose I/O Port 3 Bit 6. The function configuration of this pin is determined by programming the software configuration registers.
121	FAN_CTL4/ VID_TURBO	DOD8/ DI	VCC	Fan Control Output 4 / VID Turbo Output Enable <ul style="list-style-type: none"> The first function of this pin is Fan Control Output 4. (PWM output signal to Fan's FET.) The second function of this pin is to enable VID turbo output. The function configuration of this pin is determined by programming the software configuration registers.

Pin(s) No.	Symbol	Attribute	Power	Description
2	PSI_L/ FAN_CTL5/ CIRRX2/ GP16	DI/ DOD8/ DI/ DIDO8	VCC	PSI_L / Fan Control Output 5 / Consumer Infrared Receive Input 2 / General Purpose I/O 16. <ul style="list-style-type: none"> The first function of this pin is SVID's PSI_L input The second function of this pin is Fan Control Output 5. (PWM output signal to Fan's FET.) The third function of this pin is Consumer Infrared Receive Input 2. The fourth function of this pin is the General Purpose I/O Port 1 Bit 6 The function configuration of this pin is determined by programming the software configuration registers.

Table 5-6. Pin Description of Infrared Port Signals

Pin(s) No.	Symbol	Attribute	Power	Description
30	RESETCON#/ CIRTX1/ CE_N	DI/ DOD8/ DOD8	VCC	Reset Connect # / Consumer Infrared Transmit Output 1 / Serial Flash Chip Enable. <ul style="list-style-type: none"> The first function of this pin is Reset Connect #. It is connected to the reset button, and also to the other reset sources on the motherboard. The second function of this pin is Consumer Infrared Transmit Output 1. The third function of this pin is the Serial Flash Chip Enable. The function configuration of this pin is determined by programming the software configuration registers.
85	RSMRST#/ CIRRX1/ GP55	DOD8/ DI/ DIOD8	VCCH	Resume Reset # / Consumer Infrared Receive Input 1 / General Purpose I/O 55. <ul style="list-style-type: none"> The first function of this pin is Resume Reset #. It is a power good signal of VCCH. The high threshold is $4V \pm 0.2V$, and the low threshold is $3.5V \pm 0.2V$. The second function of this pin is Consumer Infrared Receive Input 1. The third function of this pin is the General Purpose I/O Port 5 Bit 5. The function configuration of this pin is determined by programming the software configuration registers.
3	SVD / PCIRSTIN# / CIRTX2/ GP15	DOD8/ DI/ DOD8/ DIOD8	VCC	Serial VID Data / PCI Reset Input # / Consumer Infrared Transmit Output 2 / General Purpose I/O 15. <ul style="list-style-type: none"> The first function of this pin is Serial VID Data output The second function of this pin is the PCI Reset Input #. The third function of this pin is Consumer Infrared Transmit Output 2. The fourth function of this pin is the General Purpose I/O Port 1 Bit 5 The function configuration of this pin is determined by programming the software configuration registers.
2	PSI_L/ FAN_CTL5/ CIRRX2/ GP16	DI/ DOD8/ DOD8/ DIOD8	VCC	Serial-VID PSI_L Input / Fan Control Output 5 / Consumer Infrared Receive Input 2 / General Purpose I/O 16. <ul style="list-style-type: none"> The first function of this pin is Serial-VID PSI_L input The second function of this pin is Fan Control Output 5. (PWM output signal to Fan's FET.) The third function of this pin is Consumer Infrared Receive Input 2. The fourth function of this pin is the General Purpose I/O Port 1 Bit 6 The function configuration of this pin is determined by programming the software configuration registers.

Pin(s) No.	Symbol	Attribute	Power	Description
70	GP46/ IRRX	DIOD8/ DI	VCCH	General Purpose I/O 46 / Infrared Receive Input <ul style="list-style-type: none"> The first function of this pin is the General Purpose I/O Port 4 Bit 6. The second function of this pin is Infrared Receive Input. The function configuration of this pin is determined by programming the software configuration registers.
66	IRTX/ GP47	DO8/ DIOD8	VCC	Infrared Transmit Output / General Purpose I/O 47 / Serial Flash Chip Enable 2. <ul style="list-style-type: none"> The first function of this pin is Infrared Transmit output. The second function of this pin is the General Purpose I/O Port 4 Bit 7.

Table 5-7. Pin Description of Serial Port 1 Signals

Pin(s) No.	Symbol	Attribute	Power	Description
128	RI1#	DI	VCC	Ring Indicator 1 #. When the signal is low, it indicates that a telephone ring signal has been received by the MODEM. The RI# signal is a MODEM status input whose condition can be tested by reading the MSR register.
127	DCD1#	DI	VCC	Data Carrier Detect 1 #. When the signal is low, it indicates that the MODEM or data set has detected a carrier. The DCD# signal is a MODEM status input whose condition can be tested by reading the MSR register.
126	DTR1#/ JP4	DO8/ DI	VCC	Data Terminal Ready 1 #. DTR# is used to indicate to the MODEM or data set that the device is ready to exchange data. DTR# is activated by setting the appropriate bit in the MCR register to 1. After a Master Reset operation or during Loop mode, DTR# is set to its inactive state. During LRESET#, this pin is input for JP1 power-on strapping option.
125	SIN1	DI	VCC	Serial Data Input 1. This input receives serial data from the communications link.
124	SOUT1/ JP3	DO8/ DI	VCC	Serial Data Output 1. This output sends serial data to the communications link. This signal is set to a marking state (logic 1) after a Master Reset operation or when the device is in one of the Infrared communications modes. During LRESET#, this pin is input for JP3 power-on strapping option.
123	DSR1#	DI	VCC	Data Set Ready 1 #. When the signal is low, it indicates that the MODEM or data set is ready to establish a communications link. The DSR# signal is a MODEM status input whose condition can be tested by reading the MSR register.
122	RTS1#/ JP2	DO8/ DI	VCC	Request to Send 1 #. When this signal is low, this output indicates to the MODEM or data set that the device is ready to send data. RTS# is activated by setting the appropriate bit in the MCR register to 1. After a Master Reset operation or during Loop mode, RTS# is set to its inactive state. During LRESET#, this pin is input for JP2 power-on strapping option.
1	CTS1#	DI	VCC	Clear to Send 1 #. When the signal is low, it indicates that the MODEM or data set is ready to accept data. The CTS# signal is a MODEM status input whose condition can be tested by reading the

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Pin(s) No.	Symbol	Attribute	Power	Description
				MSR register.

Table 5-8. Pin Description of Parallel Port Signals

Pin(s) No.	Symbol	Attribute	Power	Description
100	SLCT/GP80	DI	VCC	Printer Select / General Purpose I/O 80. <ul style="list-style-type: none"> The first function of this pin is Printer Select. This signal goes high when the line printer has been selected. The second function of this pin is the General Purpose I/O Port 8 Bit 1.
101	PE/ GP81	DI/ DIOD24	VCC	Printer Paper End / General Purpose I/O 81. <ul style="list-style-type: none"> The first function of this pin is Printer Paper End . This signal is set high by the printer when it runs out of paper. The second function of this pin is the General Purpose I/O Port 8 Bit 1. The function configuration of this pin is determined by programming the software configuration registers (It will be PE when LDN3 (parallel port) is enabled. Otherwise, GP80)
102	BUSY/ GP82	DI/ DIOD24	VCC	Printer Busy / General Purpose I/O 82. <ul style="list-style-type: none"> The first function of this pin is Printer Busy. This signal goes high when the line printer has a local operation in progress and cannot accept data. The second function of this pin is the General Purpose I/O Port 8 Bit 2. The function configuration of this pin is determined by programming the software configuration registers (It will be BUSY when LDN3 (parallel port) is enabled. Otherwise, GP81)
103	ACK#/ GP83	DI/ DIOD24	VCC	Printer Acknowledge # / General Purpose I/O 83. <ul style="list-style-type: none"> The first function of this pin is Printer Acknowledge #. This signal goes low to indicate that the printer has already received a character and is ready to accept another one. The second function of this pin is the General Purpose I/O Port 8 Bit 3. The function configuration of this pin is determined by programming the software configuration registers (It will be ACK# when LDN3 (parallel port) is enabled. Otherwise, GP82)
104	SLIN#/ GP84/ SMBD_R	DIO24/ DIOD24/ BI	VCC	Printer Select Input # / General Purpose I/O 84 / SMBUS Isolation <ul style="list-style-type: none"> The first function of this pin is Printer Select Input #. When the signal is low, the printer is selected. This signal is derived from the complement of bit 3 of the printer control register. The second function of this pin is the General Purpose I/O Port 8 Bit 4. The third function of this pin is SMBUS isolation circuit The function configuration of this pin is determined by programming the software configuration registers. (It will be SLIN# when LDN3 (parallel port) is enabled. Otherwise, GP83)
105	INIT#/ GP85/ SMBD_M	DIO24/ DIOD24/ BI	VCC	Printer Initialize # / General Purpose I/O 85 / SMBUS Isolation <ul style="list-style-type: none"> The first function of this pin is Printer Initialize #. When the signal is low, the printer is selected. This signal is derived from the complement of bit 3 of the printer control register. The second function of this pin is the General Purpose I/O Port 8 Bit 5. The third function of this pin is SMBUS isolation circuit The function configuration of this pin is determined by programming the software configuration registers (It will be INIT# when LDN3 (parallel port) is enabled. Otherwise, GP84)

Pin(s) No.	Symbol	Attribute	Power	Description
106	ERR#	DI/	VCC	<p>Printer Error #.</p> <ul style="list-style-type: none"> The first function of this pin is Printer Error #. When the signal is low, it indicates that the printer has encountered an error. The error message can be read from bit 3 of the printer status register. <p>The function configuration of this pin is determined by programming the software configuration registers (It will be ERR# when LDN3 (parallel port) is enabled).</p>
107	AFD#/ GP86/ SMBC_R	DIO24/ DIOD24 BI	VCC	<p>Printer Auto Line Feed # / General Purpose I/O 86 / SMBUS Isolation</p> <ul style="list-style-type: none"> The first function of this pin is Printer Auto Line Feed #. When the signal is low, it is derived from the complement of bit 1 of the printer control register and is used to advance one line after each line is printed. The second function of this pin is the General Purpose I/O Port 8 Bit 6. The third function of this pin is SMBUS isolation circuit <p>The function configuration of this pin is determined by programming the software configuration registers (It will be AFD# when LDN3 (parallel port) is enabled. Otherwise, GP86)</p>
108	STB#/ GP87/ SMBC_M	DI/ DIOD24/ BI	VCC	<p>Printer Strobe # / General Purpose I/O 87 / SMBUS Isolation</p> <ul style="list-style-type: none"> The first function of this pin is Printer Strobe 3. When the signal is low, it is the complement of bit 0 of the printer control register and is used to strobe the printing data into the printer. The second function of this pin is the General Purpose I/O Port 8 Bit 7. The third function of this pin is SMBUS isolation circuit <p>The function configuration of this pin is determined by programming the software configuration registers (It will be STB# when LDN3 (parallel port) is enabled. Otherwise, GP87)</p>
109-116	PD[0:7]/ GP7[0:7]	DIO24/ DIOD24	VCC	<p>Parallel Port Data [0:7] / General Purpose I/O 7[0:7].</p> <ul style="list-style-type: none"> The first function of these pins is Parallel Port Data [0:7]. This bus provides a byte-wide input or output to the system. The eight lines are held in a high impedance state when the port is deselected. The second function of this pin is the General Purpose I/O Port 8. <p>The function configuration of these pins is determined by programming the software configuration registers (They will be PD[0:7] when LDN3 (parallel port) is enabled. Otherwise, GP7[0:7])</p>

Table 5-9. Pin Description of Floppy Disk Controller Signals

Pin(s) No.	Symbol	Attribute	Power	Description
51	DENSEL#	DO24L	VCC	FDD Density Select #. DENSEL# is high for high data rates (500 Kbps, 1 Mbps). DENSEL# is low for low data rates (250 Kbps, 300 Kbps).
52	MTRA#	DO24L	VCC	FDD Motor A Enable #. This signal is active low.
53	SST/ AMDTSI_D/ PECI_AVA/ MTRB#	SST DIOD24/ PECI/ DO24L	VCC	SST / External Thermal Sensor Data / PECI Available / FDD Motor B Enable #. <ul style="list-style-type: none"> The first function of this pin is SST. The second function of this pin is External Thermal Sensor Clock. (AMDTSI_D) The third function of this pin is PECI available input. The fourth function of this pin is FDD Motor B #. This signal is active low. The function configuration of this pin is determined by programming the software configuration registers. Specifically when External Thermal Sensor Host is enabled (bit<6:4> of EC Index 0Ah), this pin is selected as SST or ETS_DAT.
54	DRVA#	DO24L	VCC	FDD Drive A Enable #. This signal is active low.
55	PECI/ AMDTSI_C/ PECI_AVA/ DRVB#	PECI DIOD24/ PECI/ DO24L	VCC	PECI / External Thermal Sensor Clock / PECI AVAILABLE / FDD Drive B Enable #. <ul style="list-style-type: none"> The first function of this pin is PECI. The second function of this pin is External Thermal Sensor Clock. (AMDTSI_C) The third function of this pin is PECI_available input. The fourth function of this pin is FDD Drive B #. This signal is active low. The function configuration of this pin is determined by programming the software configuration registers. Specifically when External Thermal Sensor Host is enabled (bit<6:4> of EC Index 0Ah), this pin is selected as PECI or ETS_CLK.
56	WDATA#	DO24L	VCC	FDD Write Serial Data to the Drive #. This signal is active low.
57	DIR#	DO24L	VCC	FDD Head Direction #. Step in when this signal is low and step out when high during a SEEK operation.
58	STEP#	DO24L	VCC	FDD Step Pulse #. This signal is active low.
59	HSEL#	DO24L	VCC	FDD Head Select #. This signal is active low.
60	WGATE#	DO24L	VCC	FDD Write Gate Enable #. This signal is active low.
61	RDATA#	DI	VCC	FDD Read Disk Data #. This signal is active low. It is serial data input from FDD.
62	TRK0#	DI	VCC	FDD Track 0 #. This signal is active low. It indicates that the head of the selected drive is on track 0.
63	INDEX#	DI	VCC	FDD Index #. This signal is active low. It indicates the beginning of a disk track.
64	WPT#	DI	VCC	FDD Write Protect #. This signal is active low. It indicates that the disk of the selected drive is write-protected.
65	DSKCHG#	DI	VCC	FDD Disk Change #. This signal is active low. It senses whether the drive door has

Pin(s) No.	Symbol	Attribute	Power	Description
				been opened or a diskette has been changed.

Table 5-10. Pin Description of GPIO function

Pin(s) No.	Symbol	Attribute	Power	Description
31	SVC/ PECI_RQT/ GP14	DOD8/ PECI/ DIOD8	VCC	Serial VID Clock / Peci Request / General Purpose I/O 14. <ul style="list-style-type: none"> The first function of this pin is Serial VID Clock output. The second function of this pin is Peci request output. The third function of this pin is the General Purpose I/O Port 1 Bit 4. The function configuration of this pin is determined by programming the software configuration registers.
32	PWROK1/ GP13	DOD8/ DIOD8	VCC	Power OK 1 of VCC / General Purpose I/O 13. <ul style="list-style-type: none"> The first function of this pin is Power OK 1 of VCC. The second function of this pin is the General Purpose I/O Port 1 Bit 3. The function configuration of this pin is determined by programming the software configuration registers.
33	PCIRST1#/ GP12	DOD8/ DIOD8	VCC	PCI Reset 1 # / General Purpose I/O 12. <ul style="list-style-type: none"> The first function of this pin is PCI Reset 1 #. It is a buffer of LRESET#. The second function of this pin is the General Purpose I/O Port 1 Bit 2. The function configuration of this pin is determined by programming the software configuration registers.
34	PCIRST2#/ GP11	DOD8/ DIOD8	VCC	PCI Reset 2 # / General Purpose I/O 11. <ul style="list-style-type: none"> The first function of this pin is PCI Reset 2 #. It is a buffer of LRESET#. It is a buffer output of LRESET# if bit1 of Index 2Ch is 0. It will be (LRESET# AND PCIRSTIN#) if bit1 of Index 2Ch is 1. The second function of this pin is the General Purpose I/O Port 1 Bit 1. The function configuration of this pin is determined by programming the software configuration registers.
84	PCIRST3#/ GP10/ VDIMM_STR_ EN	DOD8/ DIOD8/ DOD8	VCCH	PCI Reset 3 # / General Purpose I/O 10 / VDIMM STR Enable. <ul style="list-style-type: none"> The first function of this pin is PCI Reset 3 #. It is a buffer of LRESET#. The second function of this pin is the General Purpose I/O Port 1 Bit 0. The third function of this pin is to enable the PWM for VDIMM_STR dual voltage. The external pull high resistor is required. The function configuration of this pin is determined by programming the software configuration registers.

Table 5-11. Pin Description of Keyboard Controller Signals

Pin(s) No.	Symbol	Attribute	Power	Description
80	KDAT/ GP61	DIOD24/ DIOD24	VCCH	Keyboard Data/ General Purpose I/O 61. <ul style="list-style-type: none"> The first function of this pin is Keyboard Data. The second function of this pin is the General Purpose I/O Port 6 Bit 1. This set only supports Simple I/O function. The function configuration of this pin is determined by programming the software configuration registers. This pin doesn't support internal pull-up.
81	KCLK/ GP60	DIOD24/ DIOD24	VCCH	Keyboard Clock/ General Purpose I/O 60. <ul style="list-style-type: none"> The first function of this pin is Keyboard Clock. The second function of this pin is the General Purpose I/O Port 6 Bit 0. This set only supports Simple I/O function. The function configuration of this pin is determined by programming the software configuration registers. This pin doesn't support internal pull-up.
82	MDAT/ GP57	DIOD24/ DIOD24	VCCH	PS/2 Mouse Data/ General Purpose I/O 57. <ul style="list-style-type: none"> The first function of this pin is PS/2 Mouse Data. The second function of this pin is the General Purpose I/O Port 5 Bit 7. The function configuration of this pin is determined by programming the software configuration registers. This pin doesn't support internal pull-up.
83	MCLK/ GP56	DIOD24/ DIOD24	VCCH	PS/2 Mouse Clock / General Purpose I/O 56. <ul style="list-style-type: none"> The first function of this pin is PS/2 Mouse Clock. The second function of this pin is the General Purpose I/O Port 5 Bit 6. The function configuration of this pin is determined by programming the software configuration registers. This pin doesn't support internal pull-up.
45	KRST#/ GP62	DO16/ DIOD16	VCC	Keyboard Reset #/ General Purpose I/O 62. <ul style="list-style-type: none"> The first function of this pin is Keyboard Reset #. The second function of this pin is the General Purpose I/O Port 6 Bit 2. This set only supports Simple I/O function. The function configuration of this pin is determined by programming the software configuration registers.
46	GA20/ JP5	DO16/ DI	VCC	Gate Address 20 / Power-On Strapping 5. During LRESET#, this pin is input for JP5 power-on strapping option.

Table 5-12. Pin Description of Miscellaneous Signals

Pin(s) No.	Symbol	Attribute	Power	Description
49	CLKIN	DI	VCC	24 or 48 MHz Clock Input.
72	PWRON#/ GP44	DOD8/ DIOD8	VCCH	Power On Request Output # / General Purpose I/O44. <ul style="list-style-type: none"> The first function of this pin is Power On Request Output #. The second function of this pin is the General Purpose I/O Port 4 Bit 4. The function configuration of this pin is determined by programming the software configuration registers.
75	PANSWH#/ GP43	DI/ DIOD8	VCCH	Main Power Switch Button Input # / General Purpose I/O 43. <ul style="list-style-type: none"> The first function of this pin is Main Power Switch Button Input #. The second function of this pin is the General Purpose I/O Port 4 Bit 3. The function configuration of this pin is determined by programming the software configuration registers.
76	PSON#/ GP42	DOD8/ DIOD8	VCCH	Power Supply On-Off Output # / General Purpose I/O 42. <ul style="list-style-type: none"> The first function of this pin is Power Supply On-Off Control Output #. The second function of this pin is the General Purpose I/O Port 4 Bit 2. The function configuration of this pin is determined by programming the software configuration registers.
71	SUSB#	DI	VCCH	SUSB # Input. <ul style="list-style-type: none"> The function of this pin is SUSB # Input.
77	SUSC#/ GP53	DI/ DIOD8	VCCH	SUSC# Input / General Purpose I/O 53. <ul style="list-style-type: none"> The first function of this pin is SUSC# Input. The second function of this pin is the General Purpose I/O Port 5 Bit 3. The function configuration of this pin is determined by programming the software configuration registers.
78	PWROK2/ GP41	DOD8/ DIOD8	VCCH	Power OK 2 of VCC / General Purpose I/O 41. <ul style="list-style-type: none"> The first function of this pin is Power OK 2 of VCC. The second function of this pin is the General Purpose I/O Port 4 Bit 1. The function configuration of this pin is determined by programming the software configuration registers.
79	3VSBSW#/ GP40	DO8/ DIOD8	VCCH	3VSBSW# / General Purpose I/O 40. <ul style="list-style-type: none"> The first function of this pin is 3VSBSW#. The second function of this pin is the General Purpose I/O Port 4 Bit 0. The function configuration of this pin is determined by programming the software configuration registers.

Note 1: In addition to providing a highly integrated chip, ITE has also implemented a “SmartGuardian Utility” hardware monitoring application, providing a total solution for customers. The “SmartGuardian Utility” and the application note on the hardware monitoring circuit (the functional arrangement of VIN0-6, TMPIN1-3, FAN_TAC1-5 and FAN_CTL1-5) are interdependent. That is to say, the “SmartGuardian Utility” is accurate only when programmed according to the application note on the hardware monitoring circuit. ITE strongly recommends customers follow the referenced application circuit of IT8720F to reduce the “time-to-market” schedule.

Pin No.	Symbol	Recommended function arrangement
98	VIN0	2 Volt for VCORE1 of CPU
97	VIN1	2 Volt for VCORE2 of CPU
96	VIN2	3.3 Volt for system
95	VIN3	5 Volt for system
94	VIN4	+12 Volt for system
93	VIN5	-12 Volt for system
92	VIN6	-5 Volt for system

IO Cell:

DO8: 8mA Digital Output buffer

DOD8: 8mA Digital Open-Drain Output buffer

DO16: 16mA Digital Output buffer

DO24: 24mA Digital Output buffer

DO24L: 24mA sink/8mA drive Digital Output buffer

DIO8: 8mA Digital Input/Output buffer

DIOD8: 8mA Digital Open-Drain Input/Output buffer

DIO16: 16mA Digital Input/Output buffer

DIOD16: 16mA Digital Open-Drain Input/Output buffer

DIO24: 24mA Digital Input/Output buffer

DIOD24: 24mA Digital Open-Drain Input/Output buffer

DI: Digital Input

AI: Analog Input

AO: Analog Output

SST: special design for SST interface

PECI: special design for Peci interface

6. List of GPIO Pins

Table 6-1. General Purpose I/O Group 1 (Set 1)

Pin(s) No.	Symbol	Attribute	Description
84	PCIRST3#/ GP10/ VDIMM_STR_ EN	DOD8/ DIOD8/ DOD8	PCI Reset 3 # / General Purpose I/O 10 / VDIMM_STR Enable.
34	PCIRST2#/ GP11	DOD8/ DIOD8	PCI Reset 2 # / General Purpose I/O 11.
33	PCIRST1#/ GP12	DOD8/ DIOD8	PCI Reset 1 # / General Purpose I/O 12.
32	PWROK1/ GP13	DOD8/ DIOD8	Power OK 1 of VCC / General Purpose I/O 13.
31	SVC/ PECI_RQT/ GP14	DOD8/ PECI/ DIOD8	Serial VID Clock / PECI Request / General Purpose I/O 14.
3	SVD / PCIRSTIN# / CIRTX2/ GP15	DOD8/ DI/ DOD8/ DIOD8	SVD / PCI Reset Input # / Consumer Infrared Transmit Output 2 / General Purpose I/O 15.
2	PSI_L/ FAN_CTL5/ CIRRX2/ GP16	DI/ DOD8/ DOD8/ DIOD8	Serial-VID PSI_L Input / Fan Control Output 5 / Consumer Infrared Receive Input 2 / General Purpose I/O 16.
28	VIDO6/ GP17/ RI2#	DOD8/ DIOD8/ DI	VID Output 6 / General Purpose I/O 17 / Ring Indicator 2 #.

Table 6-2. General Purpose I/O Group 2 (Set 2)

Pin(s) No.	Symbol	Attribute	Description
27	VIDO0/ GP20/ CTS2#	DOD8/ DIOD8/ DI	VID Output 0 / General Purpose I/O 20 / Clear to Send 1 #.
26	VIDO1/ GP21/ DCD2#	DOD8/ DIOD8/ DO8	VID Output 1 / General Purpose I/O 21 / Data Carrier Detect 2 #.
25	GP22/ SCK	DI/ DIOD8	General Purpose I/O 22 / Serial Flash Clock.
24	GP23/ SI	DI/ DIOD8	General Purpose I/O 23 / Serial Flash In Data.
23	VIDO2/ FAN_TAC5/ GP24/ RTS2#	DOD8/ DI/ DIOD8/ DO8	VID Output 2 / FAN_TAC input set 5 / General Purpose I/O 24 / Request to Send 2 #.
22	VIDO3/ FAN_TAC4/ GP25/ DSR2#	DOD8/ DI/ DIOD8/ DI	VID Output 3 / FAN_TAC input set 5 / General Purpose I/O 25 / Data Set Ready 2#.
21	VIDO4/ GP26/ SOUT2	DOD8/ DIOD8/ DO8	VID Output 4 / General Purpose I/O 26 / Serial Data Output 2.
20	VIDO5/ GP27/ SIN2	DOD8/ DIOD8/ DI	VID Output 5 / General Purpose I/O 27 / Serial Data Input 2.

Table 6-3. General Purpose I/O Group 3 (Set 3)

Pin(s) No.	Symbol	Attribute	Description
19	VID0/ GP30	DIO8/ DIOD8	<i>Voltage ID 0 / General Purpose I/O 30.</i>
18	VID1/ GP31	DIO8/ DIOD8	<i>Voltage ID 1 / General Purpose I/O 31.</i>
17	VID2/ GP32	DIO8/ DIOD8	<i>Voltage ID 2 / General Purpose I/O 32.</i>
16	VID3/ GP33	DIO8/ DIOD8	<i>Voltage ID 3 / General Purpose I/O 33.</i>
14	VID4/ GP34	DIO8/ DIOD8	<i>Voltage ID 4 / General Purpose I/O 34.</i>
13	VID5/ GP35	DIO8/ DIOD8	<i>Voltage ID 5 / General Purpose I/O 35.</i>
12	FAN_CTL3/ GP36	DOD8/ DIOD8	<i>Fan Control Output 3 / General Purpose I/O 36.</i>
11	FAN_TAC3/ GP37	DI/ DIOD8	<i>Fan Tachometer Input 3 / General Purpose I/O 37.</i>

Table 6-4. General Purpose I/O Group 4 (Set 4)

Pin(s) No.	Symbol	Attribute	Description
79	3VSBSW#/ GP40	DOD8/ DIOD8	<i>3VSBSW# / General Purpose I/O 40.</i>
78	PWROK2/ GP41	DOD8/ DIOD8	<i>Power OK 2 of VCC / General Purpose I/O 41.</i>
76	PSON#/ GP42	DOD8/ DIOD8	<i>Power Supply On-Off Control Output # / General Purpose I/O 42.</i>
75	PANSWH#/ GP43	DI/ DIOD8	<i>Main Power Switch Button Input # / General Purpose I/O 43.</i>
72	PWRON#/ GP44	DOD8/ DIOD8	<i>Power On Request Output # / General Purpose I/O 44.</i>
71	SUSB#	DI	<i>SUSB # Input.</i>
70	GP46/ IRRX	DI/ DIOD8	<i>General Purpose I/O 46 / Infrared Receive Input.</i>
66	IRTX/ GP47	DO8/ DIOD8/	<i>Infrared Transmit Output / General Purpose I/O 47.</i>

Table 6-5. General Purpose I/O Group 5 (Set 5)

Pin(s) No.	Symbol	Attribute	Description
48	SO/ GP50	DI/ DIOD16	Serial Flash Output Data / General Purpose I/O 50.
10	FAN_CTL2/ GP51	DOD8/ DIOD8	Fan Control Output 2 / General Purpose I/O 51.
9	FAN_TAC2/ GP52	DI/ DIOD8	Fan Tachometer Input 2 / General Purpose I/O 52.
77	SUSC#/ GP53	DI/ DIOD8	SUSC# Input / General Purpose I/O 53.
73	PME#/ GP54	DOD8/ DIOD8	Power Management Event # / General Purpose I/O 54.
85	RSMRST#/ CIRRX1/ GP55	DOD8/ DI/ DIOD8	Resume Reset # / Consumer Infrared Receive Input 1 / General Purpose I/O 55.
83	MCLK/ GP56	DIOD24/ DIOD24	PS/2 Mouse Clock/ General Purpose I/O 56.
82	MDAT/ GP57	DIOD24/ DIOD24	PS/2 Mouse Data/ General Purpose I/O 57.

Table 6-6. General Purpose I/O Group 6 (Set 6)

Pin(s) No.	Symbol	Attribute	Description
81	KCLK/ GP60	DIOD24/ DIOD24	Keyboard Clock / General Purpose I/O 60.
80	KDAT/ GP61	DIOD24/ DIOD24	Keyboard Data / General Purpose I/O 61.
45	KRST#/ GP62	DO16/ DIOD16	Keyboard Reset / General Purpose I/O 62.
6	VCORE_GOOD/ VID6/ GP63	DI/ DIO8/ DIOD8	VCORE Good / Voltage ID 6 / General Purpose I/O 63.
5	VCORE_EN/ VID7/ GP64	DOD8/ DIO8/ DIOD8	VCORE Enable / Voltage ID 7 / General Purpose I/O 64.
120	GP65/ VDDA_EN	DIOD8/ DOD8	General Purpose I/O 65 / VDDA Enable.
119	GP66/ VLDT_EN	DIOD8/ DOD8	General Purpose I/O 66 / VLDT Enable.
118	GP67/ CPU_PG	DIOD8/ DOD8	General Purpose I/O 67 / CPU Power -good.

Table 6-7. General Purpose I/O Group 7 (Set 7)

Pin(s) No.	Symbol	Attribute	Description
109	PD0/ GP70	DIO24/ DIOD8	<i>Parallel Port Data 0 / General Purpose I/O 70.</i>
110	PD1/ GP71	DIO24/ DIOD8	<i>Parallel Port Data 1 / General Purpose I/O 71.</i>
111	PD2/ GP72/ BUSSI0	DIO24/ DIOD8/ DI	<i>Parallel Port Data 2 / General Purpose I/O 72 / Bus Select Input 0.</i>
112	PD3/ GP73/ BUSSI1	DIO24/ DIOD8/DI	<i>Parallel Port Data 3 / General Purpose I/O 73 / Bus Select Input 1.</i>
113	PD4/ GP74/ BUSSI2	DIO24/ DIOD8/DI	<i>Parallel Port Data 4 / General Purpose I/O 74 / Bus Select Input 2.</i>
114	PD5/ GP75/ BUSSO0	DIO24/ DIOD8/ DO	<i>Parallel Port Data 5 / General Purpose I/O 75 / Bus Select Output 0.</i>
115	PD6/ GP76/ BUSSO1	DIO24/ DIOD8/ DO	<i>Parallel Port Data 6 / General Purpose I/O 76 / Bus Select Output 1.</i>
116	PD7/ GP77/ BUSSO2	DIO24/ DIOD8/ DO	<i>Parallel Port Data 7 / General Purpose I/O 77 / Bus Select Output 2.</i>

Table 6-8. General Purpose I/O Group 8 (Set 8)

Pin(s) No.	Symbol	Attribute	Description
101	SLCT/ GP80	DI/ DIOD8	<i>Printer Select / General Purpose I/O 80.</i>
102	PE/ GP81	DI/ DIOD8	<i>Printer Paper End / General Purpose I/O 81.</i>
103	BUSY/ GP82	DI/ DIOD8	<i>Printer Busy / General Purpose I/O 82.</i>
104	ACK#/ GP83	DIO24/ DIOD8	<i>Printer Acknowledge # / General Purpose I/O 83.</i>
105	SLIN#/ GP84	DIO24/ DIOD8	<i>Printer Select Input # / General Purpose I/O 84.</i>
106	INIT#/ GP85	DI/ DIOD8	<i>Printer Initialize # / General Purpose I/O 85.</i>
107	AFD#/ GP86	DIO24/ DIOD8	<i>Printer Auto Line Feed # / General Purpose I/O 86.</i>
108	STB#/ GP87	DI/ DIOD8	<i>Printer Strobe # / General Purpose I/O 87.</i>

7. Power On Strapping Options and Special Pin Routings

Table 7-1. Power On Strapping Options

	Symbol	Value	Description
JP1 Pin 38	Flashseg1_EN	1	Disabled
		0	Flash I/F Address Segment FFF8_0000~FFFF_FFFF & 000E_0000~000F_FFFF is enabled.
JP2 Pin 122	VIDO_EN	1	Disable VID output pins
		0	Enable VID output pins
JP3 Pin 124	CHIP_SEL	1	Used for chip 1 when two IT8712F exist in the same system. Chip is selected in conjunction with "Global Configuration Register - Index 22, bit 7. See note in "Configuration Select and Chip Version (Index=22h) bit 7".
		0	Used for chip 0 when two IT8712F exist in the same system. Chip is selected in conjunction with "Global Configuration Register - Index 22, bit 7. See note in "Configuration Select and Chip Version (Index=22h) bit 7".
JP4 Pin 126	K8PWR_EN	1	K8 power sequence function is enabled.
		0	K8 power sequence function is disabled.
[JP3,JP5] Pin 124 & 46	FAN_CTL_SEL	11	The default value of EC Index 15h/16h/17h is 00h.
		10	The default value of EC Index 15h/16h/17h is 40h.
		01	The default value of EC Index 15h/16h/17h is 20h.
		00	The default value of EC Index 15h/16h/17h is 7Fh.
JP5 Pin 46	WDT_EN	1	Disable WDT to rest PWROK
		0	Enable WDT to rest PWROK
JP6 Pin 29	SVID_EN	1	Parallel VID Output (Only for Parallel VID Input)
		0	Serial VID Output (Only for Parallel VID Input)

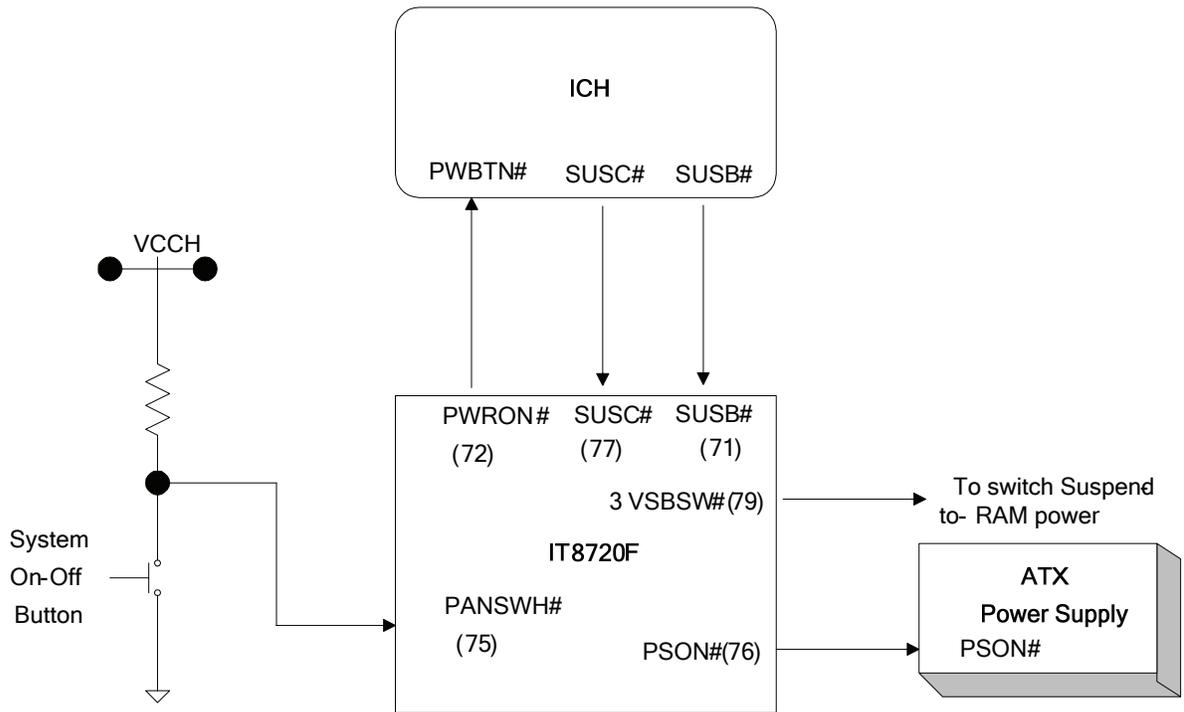
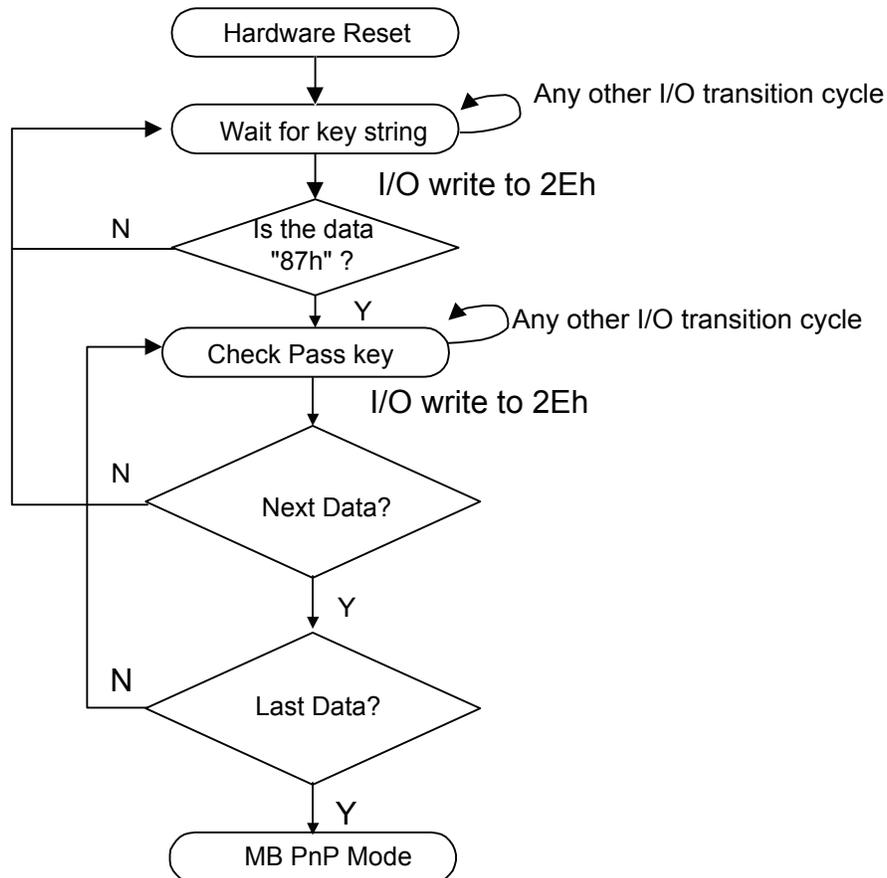


Figure 7-1. IT8720F Special Applications Circuitry for Intel ICH

8. Configuration

8.1 Configuring Sequence Description

After a hardware reset or power-on reset, the IT8720F enters the normal mode with all logical devices disabled except KBC. The initial state (enable bit) of this logical device (KBC) is "1".



There are three steps to completing the configuration setup: (1) Enter the MB PnP Mode; (2) Modify the data of configuration registers; (3) Exit the MB PnP Mode. The undesired result may occur if the MB PnP Mode is not exited properly.

(1) Enter the MB PnP Mode

To enter the MB PnP Mode, four special I/O write operations are to be performed during the Wait for Key state. To ensure the initial state of the key-check logic, it is necessary to perform four write operations to the Special Address port (2Eh). Two different enter keys are provided to select configuration ports (2Eh/2Fh or 4Eh/4Fh) of the next step.

	Address port	Data port
87h, 01h, 55h, 55h;	2Eh	2Fh
or 87h, 01h, 55h, AAh;	4Eh	4Fh

(2) Modify the Data of the Registers

All configuration registers can be accessed after entering the MB PnP Mode. Before accessing a selected register, the content of Index 07h must be changed to the LDN to which the register belongs, except some Global registers.

(3) Exit the MB PnP Mode

Set bit 1 of the configure control register (Index=02h) to “1” to exit the MB PnP Mode.

Description of the Configuration Register

All the registers except APC/PME registers will be reset to the default state when RESET is activated.

8.2 Description of the Configuration Registers

All the registers except APC/PME' registers will be reset to the default state when RESET is activated.

Table 8-1. Global Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
All	02h	W	NA	Configure Control
All	07h	R/W	NA	Logical Device Number (LDN)
All	20h	R	87h	Chip ID Byte 1
All	21h	R	20h	Chip ID Byte 2
All	22h	W-R	00h	Configuration Select and Chip Version
All	23h	R/W	00h	Clock Selection Register
All	24h	R/W	00h	Software Suspend and Flash I/F Control Register
07h ^{Note1}	25h	R/W	01h	GPIO Set 1 Multi-Function Pin Selection Register Bit 0 powered by VCCH.
07h ^{Note1}	26h	R/W	FFh	GPIO Set 2 Multi-Function Pin Selection Register Bit 0-7 powered by VCCH.
07h ^{Note1}	27h	R/W	00h	GPIO Set 3 Multi-Function Pin Selection Register
07h ^{Note1}	28h	R/W	40h	GPIO Set 4 Multi-Function Pin Selection Register Bit 0-7 powered by VCCH.
07h ^{Note1}	29h	R/W	00h	GPIO Set 5 Multi-Function Pin Selection Register Bit 3-5 powered by VCCH.
07h ^{Note1}	2Ah	R/W	00h	Extended 1 Multi-Function Pin Selection Register Bit 0-7 powered by VCCH.
All	2Bh	R/W	00h	Logical Block Configuration Lock Register
07h ^{Note1}	2Ch	R/W	03h	Extended 2 Multi-Function Pin Selection Register Bit 0-7 powered by VCCH.
F4h ^{Note1}	2Eh	R/W	00h	Test 1 Register
F4h ^{Note1}	2Fh	R/W	00h	Test 2 Register

Table 8-2. FDC Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
00h	30h	R/W	00h	FDC Activate
00h	60h	R/W	03h	FDC Base Address MSB Register
00h	61h	R/W	F0h	FDC Base Address LSB Register
00h	70h	R/W	06h	FDC Interrupt Level Select
00h	74h	R/W	02h	FDC DMA Channel Select
00h	F0h	R/W	00h	FDC Special Configuration Register 1
00h	F1h	R/W	00h	FDC Special Configuration Register 2

Table 8-3. Serial Port 1 Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
01h	30h	R/W	00h	Serial Port 1 Activate
01h	60h	R/W	03h	Serial Port 1 Base Address MSB Register
01h	61h	R/W	F8h	Serial Port 1 Base Address LSB Register
01h	70h	R/W	04h	Serial Port 1 Interrupt Level Select
01h	F0h	R/W	00h	Serial Port 1 Special Configuration Register 1
01h	F1h	R/W	50h	Serial Port 1 Special Configuration Register 2

Table 8-4. Serial Port 2 Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
02h	30h	R/W	00h	Serial Port 2 Activate
02h	60h	R/W	02h	Serial Port 2 Base Address MSB Register
02h	61h	R/W	F8h	Serial Port 2 Base Address LSB Register
02h	70h	R/W	03h	Serial Port 2 Interrupt Level Select
02h	F0h	R/W	00h	Serial Port 2 Special Configuration Register 1
02h	F1h	R/W	50h	Serial Port 2 Special Configuration Register 2

Table 8-5. Parallel Port Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
03h	30h	R/W	00h	Parallel Port Activate
03h	60h	R/W	03h	Parallel Port Primary Base Address MSB Register
03h	61h	R/W	78h	Parallel Port Primary Base Address LSB Register
03h	62h	R/W	07h	Parallel Port Secondary Base Address MSB Register
03h	63h	R/W	78h	Parallel Port Secondary Base Address LSB Register
03h	70h	R/W	07h	Parallel Port Interrupt Level Select
03h	74h	R/W	03h	Parallel Port DMA Channel Select ^{Note2}
03h	F0h	R/W	03h ^{Note3}	Parallel Port Special Configuration Register

Table 8-6. Environment Controller Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
04h	30h	R/W	00h	Environment Controller Activate
04h	60h	R/W	02h	Environment Controller Base Address MSB Register
04h	61h	R/W	90h	Environment Controller Base Address LSB Register
04h	62h	R/W	02h	PME Direct Access Base Address MSB Register
04h	63h	R/W	30h	PME Direct Access Base Address LSB Register
04h	70h	R/W	09h	Environment Controller Interrupt Level Select
04h	F0h	R/W	00h	APC/PME Event Enable Register
04h	F1h	R/W	00h	APC/PME Status Register
04h	F2h	R/W	00h	APC/PME Control Register 1
04h	F3h	R/W	00h	Environment Controller Special Configuration Register
04h	F4h	R-R/W	00h	APC/PME Control Register 2
04h	F5h	R/W	-	APC/PME Special Code Index Register
04h	F6h	R/W	-	APC/PME Special Code Data Register

Table 8-7. KBC(Keyboard) Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
05h	30h	R/W	01h	KBC Activate
05h	60h	R/W	00h	KBC Data Base Address MSB Register
05h	61h	R/W	60h	KBC Data Base Address LSB Register
05h	62h	R/W	00h	KBC Command Base Address MSB Register
05h	63h	R/W	64h	KBC Command Base Address LSB Register
05h	70h	R/W	01h	KBC Interrupt Level Select
05h	71h	R-R/W	02h	KBC Interrupt Type ^{Note5}
05h	F0h	R/W	48h	KBC Special Configuration Register

Table 8-8. KBC(Mouse) Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
06h	30h	R/W	00h	KBC (Mouse) Activate
06h	70h	R/W	0Ch	KBC (Mouse) Interrupt Level Select
06h	71h	R-R/W	02h	KBC (Mouse) Interrupt Type ^{Note4}
06h	F0h	R/W	00h	KBC (Mouse) Special Configuration Register

Table 8-9. GPIO Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
07h	60h	R/W	00h	SMI# Normal Run Access Base Address MSB Register
07h	61h	R/W	00h	SMI# Normal Run Access Base Address LSB Register
07h	62h	R/W	00h	Simple I/O Base Address MSB Register

LDN	Index	R/W	Reset	Configuration Register or Action
07h	63h	R/W	00h	Simple I/O Base Address LSB Register
07h	64h	R/W	00h	Serial Flash I/F Base Address MSB Register
07h	65h	R/W	00h	Serial Flash I/F Base Address LSB Register
07h	70h	R/W	00h	Panel Button De-bounce Interrupt Level Select Register
07h	71h	R/W	00h	Watch Dog Timer Control Register
07h	72h	R/W	001s0000b	Watch Dog Timer Configuration Register
07h	73h	R/W	38h	Watch Dog Timer Time-out Value (LSB) Register
07h	74h	R/W	00h	Watch Dog Timer Time-out Value (MSB) Register
07h	B0h	R/W	00h	GPIO Set 1 Pin Polarity Register
07h	B1h	R/W	00h	GPIO Set 2 Pin Polarity Register
07h	B2h	R/W	00h	GPIO Set 3 Pin Polarity Register
07h	B3h	R/W	00h	GPIO Set 4 Pin Polarity Register
07h	B4h	R/W	00h	GPIO Set 5 Pin Polarity Register
07h	B5h	R/W	00h	GPIO Set 6 Pin Polarity Register
07h	B8h	R/W	20h	GPIO Set 1 Pin Internal Pull-up Enable Register
07h	B9h	R/W	00h	GPIO Set 2 Pin Internal Pull-up Enable Register
07h	BAh	R/W	00h	GPIO Set 3 Pin Internal Pull-up Enable Register
07h	BBh	R/W	00h	GPIO Set 4 Pin Internal Pull-up Enable Register
07h	BCh	R/W	00h	GPIO Set 5 Pin Internal Pull-up Enable Register
07h	BDh	R/W	00h	GPIO Set 6 Pin Internal Pull-up Enable Register
07h	C0h	R/W	01h	Simple I/O Set 1 Enable Register Bit-0 powered by VCCH.
07h	C1h	R/W	00h	Simple I/O Set 2 Enable Register Bit 0-7 powered by VCCH.
07h	C2h	R/W	00h	Simple I/O Set 3 Enable Register
07h	C3h	R/W	40h	Simple I/O Set 4 Enable Register Bit 0-7 powered by VCCH.
07h	C4h	R/W	00h	Simple I/O Set 5 Enable Register Bit 0-7 powered by VCCH.
07h	C8h	R/W	01h	Simple I/O Set 1 Output Enable Register
07h	C9h	R/W	00h	Simple I/O Set 2 Output Enable Register
07h	CAh	R/W	00h	Simple I/O Set 3 Output Enable Register
07h	CBh	R/W	40h	Simple I/O Set 4 Output Enable Register Bit 0-7 powered by VCCH.
07h	CCh	R/W	00h	Simple I/O Set 5 Output Enable Register Bit 0-7 powered by VCCH.

Table 8-10. GPIO Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
07h	E0h	R/W	00h	Panel Button De-bounce 0 Input Pin Mapping Register
07h	E1h	R/W	00h	Panel Button De-bounce 1 Input Pin Mapping Register
07h	E2h	R/W	00h	IRQ External Routing 0 Input Pin Mapping Register
07h	E3h	R/W	00h	IRQ External Routing 1 Input Pin Mapping Register
07h	E4h	R/W	00h	IRQ External Routing 1-0 Interrupt Level Selection Register
07h	E5h	R/W	00h	VID Watchdog Timer 0 Value Register
07h	E6h	R/W	00h	VID Watchdog Timer 1 Value Register
07h	E7h	R/W	00h	Reserved
07h	F0h	R/W	00h	SMI# Control Register 1
07h	F1h	R/W	00h	SMI# Control Register 2
07h	F2h	R/W	00h	SMI# Status Register 1
07h	F3h	R/W	00h	SMI# Status Register 2
07h	F4h	R/W	00h	SMI# Pin Mapping Register
07h	F5h	R/W	00h	Hardware Monitor Thermal Output Pin Mapping Register Bit 0-7 powered by VCCH.
07h	F6h	R/W	00h	Hardware Monitor Alert Beep Pin Mapping Register
07h	F7h	R/W	00h	Keyboard Lock Pin Mapping Register
07h	F8h	R/W	00h	GP LED Blinking 1 Pin Mapping Register Bit 0-7 powered by VCCH.
07h	F9h	R/W	00h	GP LED Blinking 1 Control Register Bit 0-7 powered by VCCH.
07h	FAh	R/W	00h	GP LED Blinking 2 Pin Mapping Register Bit 0-7 powered by VCCH.
07h	FBh	R/W	00h	GP LED Blinking 2 Control Register Bit 0-7 powered by VCCH.
07h	FCh	R/W-R	--h	VID Input Register
07h	FDh	R/W	00h	VID Output Register Bit 0-7 powered by VCCH.
07h	FEh	R/W	00h	VID Watchdog Timer Control Register
07h	FFh	R/W	00h	VID Watchdog Timer Control Register

Table 8-11. Consumer IR Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
0Ah	30h	R/W	00h	Consumer IR Activate
0Ah	60h	R/W	03h	Consumer IR Base Address MSB Register
0Ah	61h	R/W	10h	Consumer IR Base Address LSB Register
0Ah	70h	R/W	0Bh	Consumer IR Interrupt Level Select
0Ah	F0h	R/W	06h	Consumer IR Special Configuration Register

Note 1: All these registers can be read from all LDNs.

Note 2: When the ECP mode is not enabled, this register is **read only** as "04h", and cannot be written.

Note 3: When the bit 2 of the Primary Base Address LSB Register of Parallel Port is set to 1, the EPP mode cannot be enabled. Bit 0 of this register is always 0.

Note 4: These registers are **read only** unless the write enable bit (Index=F0h) is asserted.

8.2.1 Logical Device Base Address

The base I/O range of logical devices shown below is located in the base I/O address range of each logical device.

Table 8-12. Base Address of Logical Devices

Logical Devices	Address	Notes
LDN=0 FDC	Base + (2 - 5) and + 7	
LDN=1 SERIAL PORT 1	Base + (0 -7)	
LDN=2 SERIAL PORT 2	Base1 + (0 -7)	COM port
LDN=3 PARALLEL PORT	Base1 + (0 -3) Base1 + (0 -7) Base1 + (0 -3) and Base2 + (0 -3) Base1 + (0 -7) and Base2 + (0 -3) Base3	SPP SPP+EPP SPP+ECP SPP+EPP+ECP POST data port
LDN=4 Environment Controller	Base1 + (0 -7) Base2 + (0 -3)	Environment Controller PME#
LDN=5 KBC	Base1 + Base2	KBC
LDN=A Consumer IR	Base + (0 -7)	

8.3 Global Configuration Registers (LDN: All)

8.3.1 Configure Control (Index=02h)

This register is **write only**. Its values are not sticky; that is to say, a hardware reset will automatically clear the bits, and does not require the software to clear them.

Bit	Description
7-2	Reserved
1	Returns to the "Wait for Key" state. This bit is used when the configuration sequence is completed.
0	Resets all logical devices and restores configuration registers to their power-on states.

8.3.2 Logical Device Number (LDN, Index=07h)

This register is used to select the current logical devices. By reading from or writing to the configuration of I/O, Interrupt, DMA and other special functions, all registers of the logical devices can be accessed. In addition, ACTIVATE command is only effective for the selected logical devices. This register is **read/write**.

8.3.3 Chip ID Byte 1 (Index=20h, Default=87h)

This register is the Chip ID Byte 1 and is **read only**. Bits [7:0]=87h when read.

8.3.4 Chip ID Byte 2 (Index=21h, Default=20h)

This register is the Chip ID Byte 2 and is **read only**. Bits [7:0]=20h when read.

8.3.5 Configuration Select and Chip Version (Index=22h, Default=00h)

Bit	Description
7	Configuration Select This bit is used to select the chip to be configured. When there are two IT8720F chips in a system, and "1" is written, this bit will select the chip with JP3=1 (power-on strapping value of SOUT1) to be configured and the chip with JP3=0 will exit the configuration mode. When "0" is written, the chip with JP3=0 will be configured and the chip with JP3=1 will exit the configuration mode. If no writing operation occurs to this register, both chips will be configured.
6-4	Reserved
3-0	Version

8.3.6 Clock Selection Register (Index=23h, Default=00h)

Bit	Description
7-6	XLOCK select These two bits determine the XLOCK function. 00: Software XLOCK (default) 01: Reserved 10: Pin 48 (GP50) 11: Pin 11 (GP37)
5	Reserved
4	Clock Source Select of Watch Dog Timer 0: Internal oscillating clock (default) 1: External CLKIN

Bit	Description
3-2	Delay Select of PWOK1/2 (Powered by VSB) 00: POWOK1/2 will be delayed 300~600ms from VCC5V > 4.0V. 01: POWOK1/2 will not be delayed from VCC5V > 4.0V. 10: POWOK1/2 will be delayed 150~300ms from VCC5V > 4.0V. 11: Reserved.
1	Reserved
0	CLKIN Frequency 0: 48 MHz 1: 24 MHz

8.3.7 Software Suspend and Flash I/F Control Register (Index=24h, Default=0000s0s0b, MB PnP)

Bit	Description
7	Flash I/F Address Segment 6 (FFDF_FFFFh-FFD0_0000h) 0: Disable 1: Enable
6	Flash I/F Address Segment 5 (FFEF_FFFFh-FFE0_0000h) 0: Disable 1: Enable
5	Flash I/F Address Segment 4 (FFF7_FFFFh-FFF0_0000h) 0: Disable 1: Enable
4	LPC Memory/FWM write to Serial Flash I/F Enable 0: Disable (default) 1: Enable
3	Flash I/F Address Segment 3 (FFF8_0000h-FFFD_FFFFh, FFFE_0000h-FFFE_FFFFh) 0: Disable 1: Enable
2	Flash I/F Address Segment 2 (FFEF_0000h-FFEF_FFFFh, FFEE_0000h-FFEE_FFFFh) 0: Disable (default) 1: Enable
1	Flash I/F Address Segment 1 (FFFE_0000h-FFFF_FFFFh, 000E_0000h-000F_FFFFh) 0: Disable 1: Enable
0	Flash I/F Address Segment 7 (FFCF_FFFFh-FFC0_0000h) 0: Disable 1: Enable

8.3.8 GPIO Set 1 Multi-Function Pin Selection Register (Index=25h, Default=00h)

If the enabled bits are not set, the multi-function pins will perform the original functions. Conversely, if they are set, they will perform the GPIO functions. This register can be read from any LDN, but can only be written if LDN=07h.

Bit	Description
7	Function Selection of Pin 28 if JP2 = 1 (VIDO6 if JP2=0) 0: RI2# 1: General Purpose I/O 17 (GP17)
6	Function Selection of Pin 2 0: FAN_CTL5 if bits[3:2] of EC index 0Bh \neq 11b; CIRRX2 if bit6 of CIR IER = 1; PSI_L if bit4 of Global Index 2Ah. 1: General Purpose I/O 16 (GP16)

Bit	Description
5	Function Selection of Pin 3 0: SVD if JP6=0; or PCIRSTIN# if bit2 of index 2C is 0; or CIRTX2 if bit7 of CIR IER = 1. 1: General Purpose I/O 15 (GP15)
4	Function Selection of Pin 31 0: SVC 1: General Purpose I/O 14 (GP14)
3	Function Selection of Pin 32 0: PWROK1 1: General Purpose I/O 13 (GP13)
2	Function Selection of Pin 33 0: PCIRST1# 1: General Purpose I/O 12 (GP12)
1	Function Selection of Pin 34 0: PCIRST2# 1: General Purpose I/O 11 (GP11)
0	Function Selection of Pin 84 if K8 Power-sequence not Selected. This pin is VDIMM_STR_EN if K8 Power-sequence is selected 0: PCIRST3# 1: General Purpose I/O 10 (GP10)

8.3.9 GPIO Set 2 Multi-Function Pin Selection Register (Index=26h, Default=FFh)

If the enabled bits are not set, the multi-function pins will perform the original functions. Conversely, if they are set, they will perform the GPIO functions. This register can be read from any LDN, but can only be written if LDN=07h.

Bit	Description
7	Function Selection of Pin 20 if JP2 = 0 (VIDO5 if JP2=1) 0: SIN2 1: General Purpose I/O 27 (GP27)
6	Function Selection of Pin 21 if JP2 = 0 (VIDO4 if JP2=1) 0: SOUT2 1: General Purpose I/O 26 (GP26)
5	Function Selection of Pin 22 if JP2 = 0 (VIDO3 if JP2=1) 0: DSR2# / FAN_TAC4 1: General Purpose I/O 25 (GP25)
4	Function Selection of Pin 23 if JP2 = 0 (VIDO2 if JP2=1) 0: RTS2# / FAN_TAC5 1: General Purpose I/O 24 (GP24)
3	Function Selection of Pin 24 0: SI 1: General Purpose I/O 23 (GP23)
2	Function Selection of Pin 25 0: SCK 1: General Purpose I/O 22 (GP22)
1	Function Selection of Pin 26 if JP2 = 0 (VIDO1 if JP2=1) 0: DTR2# 1: General Purpose I/O 21 (GP21)
0	Function Selection of Pin 27 if JP2 = 0 (VIDO0 if JP2=1) 0: CTS2# 1: General Purpose I/O 20 (GP20)

8.3.10 GPIO Set 3 Multi-Function Pin Selection Register (Index=27h, Default=00h)

If the enabled bits are not set, the multi-function pins will perform the original functions. Conversely, if they are set, they will perform the GPIO functions. This register can be read from any LDN, but can only be written if LDN=07h.

Bit	Description
7	Function Selection of Pin 11 0: Fan Tachometer Input 3 (FAN_TAC3) 1: General Purpose I/O 37 (GP37)
6	Function Selection of Pin 12 0: Fan Control Output 3 (FAN_CTL3) 1: General Purpose I/O 36 (GP36)
5	Function Selection of Pin 13 0: Voltage ID5 (VID5) 1: General Purpose I/O 35 (GP35)
4	Function Selection of Pin 14 0: Voltage ID4 (VID4) 1: General Purpose I/O 34 (GP34)
3	Function Selection of Pin 16 0: Voltage ID3 (VID3) 1: General Purpose I/O 33 (GP33)
2	Function Selection of Pin 17 0: Voltage ID2 (VID2) 1: General Purpose I/O 32 (GP32)
1	Function Selection of Pin 18 0: Voltage ID1 (VID1) 1: General Purpose I/O 31 (GP31)
0	Function Selection of Pin 19 0: Voltage ID0 (VID0) 1: General Purpose I/O 30 (GP30)

8.3.11 GPIO Set 4 Multi-Function Pin Selection Register (Index=28h, Default=40h)

If the enabled bits are not set, the multi-function pins will perform the original functions. Conversely, if they are set, they will perform the GPIO functions. This register can be read from any LDN, but can only be written if LDN=07h.

Bit	Description
7	Function Selection of Pin 66 0: Infrared Transmit Output (IRTX) 1: General Purpose I/O 47 (GP47)
6	Function Selection of Pin 70 0: Infrared Receive Input (IRRX) 1: General Purpose I/O 46 (GP46)
5	Function Selection of Pin 71 0: SUSB# 1: Reserved
4	Function Selection of Pin 72 0: Power On Request Output # (PWRON#) 1: General Purpose I/O 44 (GP44)

Bit	Description
3	Function Selection of Pin 75 0: Main Power Switch Button Input # (PANSWH#) 1: General Purpose I/O 43 (GP43)
2	Function Selection of Pin 76 0: Power Supply ON-Off Control Output # (PSON#) 1: General Purpose I/O 42 (GP42)
1	Function Selection of Pin 78 0: PWROK2 1: General Purpose I/O 41 (GP41)
0	Function Selection of Pin 79 0: 3VSBSW# 1: General Purpose I/O 40 (GP40)

8.3.12 GPIO Set 5 Multi-Function Pin Selection Register (Index=29h, Default=00h)

If the enabled bits are not set, the multi-function pins will perform the original functions. Conversely, if they are set, they will perform the GPIO functions. This register can be read from any LDN, but can only be written if LDN=07h.

Bit	Description
7	Function Selection of Pin 6, 5, 120, 119, 118 0: VCORE_GOOD, VCORE_EN, VDDA_EN, VLDT_EN, CPU_PG. 1: General Purpose I/O 63, 64, 65, 66, 67.
6	Function Selection of Pin 83, 82, 81, 80, 45 0: MCLK, MDAT, KCLK, KDAT, KRST# 1: General Purpose I/O 56, 57, 60, 61, 62
5	Function Selection of Pin 85 0: Consumer Infrared Receive Input (CIRRX1) or RSMRST#. RSMRST# is an open-drain output function, which is active low about 16ms when VCCH5V is powered on. 1: General Purpose I/O 55 (GP55).
4	Function Selection of Pin 73 0: Power Management Event # (PME#) 1: General Purpose I/O 54 (GP54)
3	Function Selection of Pin 77 0: SUSC# 1: General Purpose I/O 53 (GP53)
2	Function Selection of Pin 9 0: Fan Tachometer Input 2 (FAN_TAC2) 1: General Purpose I/O 52 (GP52)
1	Function Selection of Pin 10 0: Fan Control Output 2 (FAN_CTL2) 1: General Purpose I/O 51 (GP51)
0	Function Selection of Pin 48 0: SO 1: General Purpose I/O 50 (GP50)

8.3.13 Extended 1 Multi-Function Pin Selection Register (Index=2Ah, Default=00h)

This register can be read from any LDN, but can only be written if LDN=07h.

Bit	Description
7	Enable 3VSBSW# (For System Suspend-to-RAM) 0: 3VSBSW# is always inactive. 1: 3VSBSW# is enabled. It will be (NOT SUSB#) NAND SUSC#.
6	Multi-function selection of pin 53 0: MTRB#. 1: External Thermal Sensor Data (EC index 0Ah/bit6=1 external thermal sensor host enable, pin-53 becomes ETS_DAT function.)
5	Extended multi-function selection of pin 30 0: RESETCON#/CE_N 1: CIRTX
4	Enable PSI_L (Serial VID function) of Pin 2 0: Disable (Default) 1: Enable
3	Reserved
2	Reserved
1	Reserved
0	Reserved

8.3.14 Logical Block Lock Register (Index=2Bh, Default=00h)

When the lock function is enabled (bit7=1 or XLOCK# is low), configuration registers of the selected logical block and Clock Selection register (index = 23h), and this register will be read-only.

Bit	Description
7	Software Lock Enable Once this bit is set to 1 by software, it can be only cleared by hardware reset. 0: Configuration lock is controlled by XLOCK#. (Default) 1: Configuration registers Logic Blocks are selected by bit 6-0 and this register is read-only.
6	GPIO Select (LDN7) 0: GPIO Configuration registers are programmable. 1: GPIO Configuration registers are read-only if LOCK is enabled.
5	KBC (Keyboard) and KBC (Mouse) Select (LDN5 and LDN6) 0: KBC (Keyboard) and KBC (Mouse) Configuration registers are programmable. 1: KBC (Keyboard) and KBC (Mouse) Configuration registers are read-only if LOCK is enabled.
4	EC Select (LDN4) 0: EC Configuration registers are programmable. 1: EC Configuration registers are read-only if LOCK is enabled.
3	Parallel Port Select (LDN3) 0: Parallel Port Configuration registers are programmable. 1: Parallel Port Configuration registers are read-only if LOCK is enabled.
2	Serial Port 2 Select. (LDN2) 0: Serial Port 2 Configuration registers are programmable. 1: Serial Port 2 Configuration registers are read-only if LOCK is enabled.
1	Serial Port 1 Select. (LDN1) 0: Serial Port 1 Configuration registers are programmable. 1: Serial Port 1 Configuration registers are read-only if LOCK is enabled.

Bit	Description
0	FDC Select (LDN0) The lock function will not affect bit0 of FDC Special Configuration register (software write protect). 0: FDC Configuration registers are programmable. 1: FDC Configuration registers are read-only (except Software Write Protect bit) if LOCK is enabled.

8.3.15 Extended 2 Multi-Function Pin Selection Register (Index=2Ch, Default=03h)

This register can be read from any LDN, but can only be written if LDN=07h.

Bit	Description
7	Smbus Isolation Disable 0: Enable(Default) 1: Disable
6	K8 PWRON_SEL if JP4=1 0: Normal (Default) 1: Software Disabled
5	VID_TURBO enable 0: Disable (Default) 1: Enable
4	Extended Multi-function Selection of Pin 23 0: Disable FAN_TAC set 5 (Default) 1: Enable FAN_TAC set 5
3	Extended Multi-function Selection of Pin 22 0: Disable FAN_TAC set 4 (Default) 1: Enable FAN_TAC set 4
2	Enable PCIRSTIN# of Pin 3 0: Disable(Default) 1: Enable
1	Enable Internal Voltage Divider for VCCH5V 0: Disable 1: Enable (Default)
0	Enable ATXPG (pin 95) / Switch VIN3 Function to Internal Voltage Divider for VCC5V 0: Disable 1: Enable (Default)

8.3.16 Test 1 Register (Index=2Eh, Default=00h)

This register is the Test 1 Register and is reserved for ITE. It should not be set.

8.3.17 Test 2 Register (Index=2Fh, Default=00h)

This register is the Test 2 Register and is reserved for ITE. It should not be set.

8.4 FDC Configuration Registers (LDN=00h)

8.4.1 FDC Activate (Index=30h, Default=00h)

Bit	Description
7-1	Reserved
0	FDC Enable 1: Enable 0: Disable

8.4.2 FDC Base Address MSB Register (Index=60h, Default=03h)

Bit	Description
7-4	Read only , with "0h" for Base Address [15:12].
3-0	Mapped as Base Address [11:8].

8.4.3 FDC Base Address LSB Register (Index=61h, Default=F0h)

Bit	Description
7-3	Read/write , mapped as Base Address [7:3].
2-0	Read only as "000b."

8.4.4 FDC Interrupt Level Select (Index=70h, Default=06h)

Bit	Description
7-4	Reserved with default "0h."
3-0	Select the interrupt level ^{Note1} for FDC.

8.4.5 FDC DMA Channel Select (Index=74h, Default=02h)

Bit	Description
7-3	Reserved with default "00h."
2-0	Select the DMA channel ^{Note2} for FDC.

8.4.6 FDC Special Configuration Register 1 (Index=F0h, Default=00h)

Bit	Description
7-5	Reserved with default "00h."
4	Internal Pull-up Control of FDD I/F Input Pin 0: Disable 1: Enable
3	1: IRQ sharing 0: Normal IRQ
2	1: Swap Floppy Drives A, B 0: Normal
1	1: 3-mode 0: AT-mode
0	1: Software Write Protect 0: Normal

8.4.7 FDC Special Configuration Register 2 (Index=F1h, Default=00h)

Bit	Description
7-4	Reserved with default "00h"
3-2	FDD B Data Rate Table Select (DRT1-0)
1-0	FDD A Data Rate Table Select (DRT1-0)

8.5 Serial Port 1 Configuration Registers (LDN=01h)

8.5.1 Serial Port 1 Activate (Index=30h, Default=00h)

Bit	Description
7-1	Reserved
0	Serial Port 1 Enable 1: Enable 0: Disable

8.5.2 Serial Port 1 Base Address MSB Register (Index=60h, Default=03h)

Bit	Description
7-4	Read only as "0h" for Base Address[15:12]
3-0	Read/write , mapped as Base Address[11:8]

8.5.3 Serial Port 1 Base Address LSB Register (Index=61h, Default=F8h)

Bit	Description
7-3	Read/write , mapped as Base Address[7:3]
2-0	Read only as "000b"

8.5.4 Serial Port 1 Interrupt Level Select (Index=70h, Default=04h)

Bit	Description
7-4	Reserved with default "0h"
3-0	Select Interrupt Level ^{Note1} for Serial Port 1

8.5.5 Serial Port 1 Special Configuration Register 1 (Index=F0h, Default=00h)

Bit	Description
7	Reserved
6-4	Serial Port 1 Mode ^{Note3} 000: Standard (default) 001: IrDA 1.0 (HP SIR) 010 : ASKIR else : Reserved
3	Reserved with default "0"
2-1	Clock Source 00: 24 MHz/13 (Standard) 01: 24 MHz/12 10: Reserved 11: Reserved
0	1: IRQ sharing 0: Normal

8.5.6 Serial Port 1 Special Configuration Register 2 (Index=F1h, Default=50h)

Bit	Description
7	1: No transmission is delayed (40 bits) when the SIR or ASKIR is switched from the RX mode to TX mode. 0: Transmission is delayed (40 bits) when the SIR or ASKIR is switched from the RX mode to TX mode.
6	1: No reception is delayed (40 bits) when the SIR or ASKIR is switched from the TX mode to RX mode. 0: Reception is delayed (40 bits) when the SIR or ASKIR is switched from the TX mode to RX mode.
5	Single Mask Mode When this bit is set, the RX of UART is masked under TX transmission.
4	1: Half duplex (Default) 0: Full duplex
3	SIR RX polarity 1: Active low 0: Active high
2-0	Reserved

8.6 Serial Port 2 Configuration Registers (LDN=02h)

8.6.1 Serial Port 2 Activate (Index=30h, Default=00h)

Bit	Description
7-1	Reserved
0	Serial Port 2 Enable 1: Enable 0: Disable

8.6.2 Serial Port 2 Base Address MSB Register (Index=60h, Default=02h)

Bit	Description
7-4	Read only with "0h" for Base Address [15:12]
3-0	Read/write , mapped as Base Address [11:8]

8.6.3 Serial Port 2 Base Address LSB Register (Index=61h, Default=F8h)

Bit	Description
7-3	Read/write , mapped as Base Address [7:3]
2-0	Read only as "000b"

8.6.4 Serial Port 2 Interrupt Level Select (Index=70h, Default=03h)

Bit	Description
7-4	Reserved with default "0h"
3-0	Select the interrupt level ^{Note1} for Serial Port 2

8.6.5 Serial Port 2 Special Configuration Register 1 (Index=F0h, Default=00h)

Bit	Description
7	Reserved
6-4	Serial Port 2 Mode ^{Note3} 000: Standard (default) 001: IrDA 1.0 (HP SIR) 010 : ASKIR else : Reserved
3	Reserved with default "0"
2-1	Clock Source 00: 24 MHz/13 (Standard) 01: 24 MHz/12 10: Reserved 11: Reserved
0	1: IRQ sharing 0: Normal

8.6.6 Serial Port 2 Special Configuration Register 2 (Index=F1h, Default=50h)

Bit	Description
7	1: No transmission is delayed (40 bits) when the SIR or ASKIR is switched from the RX mode to TX mode. 0: Transmission is delayed (40 bits) when the SIR or ASKIR is switched from the RX mode to TX mode.
6	1: No reception is delayed (40 bits) when the SIR or ASKIR is switched from the TX mode to RX mode. 0: Reception is delayed (40 bits) when the SIR or ASKIR is switched from the TX mode to RX mode.
5	Single Mask Mod When this bit is set, the RX of UART is masked under TX transmission.
4	1: Half duplex (Default) 0: Full duplex
3	SIR RX polarity 1: Active low 0: Active high
2-0	Reserved

8.7 Parallel Port Configuration Registers (LDN=03h)

8.7.1 Parallel Port Activate (Index=30h, Default=00h)

Bit	Description
7-1	Reserved
0	Parallel Port Enable 1: Enable 0: Disable

8.7.2 Parallel Port Primary Base Address MSB Register (Index=60h, Default=03h)

Bit	Description
7-4	Read only as "0h" for Base Address[15:12]
3-0	Read/write , mapped as Base Address[11:8]

8.7.3 Parallel Port Primary Base Address LSB Register (Index=61h, Default=78h)

If bit 2 is set to 1, the EPP mode is disabled automatically.

Bit	Description
7-2	Read/write , mapped as Base Address[7:2]
1-0	Read only as "00b"

8.7.4 Parallel Port Secondary Base Address MSB Register (Index=62h, Default=07h)

Bit	Description
7-4	Read only as "0h" for Base Address[15:12]
3-0	Read/write , mapped as Base Address[11:8]

8.7.5 Parallel Port Secondary Base Address LSB Register (Index=63h, Default=78h)

Bit	Description
7-2	Read/write , mapped as Base Address[7:2]
1-0	Read only as "00b"

8.7.6 Parallel Port Interrupt Level Select (Index =70h, Default=07h)

Bit	Description
7-4	Reserved with default "0h"
3-0	Select the interrupt level Note1 for Parallel Port

8.7.7 Parallel Port DMA Channel Select (Index=74h, Default=03h)

Bit	Description
7-3	Reserved with default "00h"
2-0	Select the DMA channel Note2 for Parallel Port

8.7.8 Parallel Port Special Configuration Register (Index=F0h, Default=0Bh)

Bit	Description
7-4	Reserved
3	1: POST Data Port Disable 0: POST Data Port Enable
2	1: IRQ sharing 0: Normal
1-0	Parallel Port Modes 00 : Standard Parallel Port mode (SPP) 01 : EPP mode 10 : ECP mode 11 : EPP mode & ECP mode

These bits are independent.

If bit 1 is set, ECP mode is enabled.

If bit 0 is set, EPP mode is enabled except when Parallel Port Primary Base Address LSB Register bit 2 is set to 1 in accordance with the EPP specification.

8.8 Environment Controller Configuration Registers (LDN=04h)

8.8.1 Environment Controller Activate Register (Index=30h, Default=00h)

Bit	Description
7-1	Reserved
0	Environment Controller Enable 1: Enable 0: Disable This is a read/write register.

8.8.2 Environment Controller Base Address MSB Register (Index=60h, Default=02h)

Bit	Description
7-4	Read only as "0h" for Base Address[15:12]
3-0	Read/write , mapped as Base Address[11:8]

8.8.3 Environment Controller Base Address LSB Register (Index=61h, Default=90h)

Bit	Description
7-3	Read/write , mapped as Base Address[7:3]
2-0	Read only as "000b"

8.8.4 PME Direct Access Base Address MSB Register (Index=62h, Default=02h)

Bit	Description
7-4	Read only as "0h" for Base Address[15:12]
3-0	Read/write , mapped as Base Address[11:8]

8.8.5 PME Direct Access Base Address LSB Register (Index=63h, Default=30h)

Bit	Description
7-3	Read/write , mapped as Base Address[7:3]
2-0	Read only as "000b."

8.8.6 Environment Controller Interrupt Level Select (Index=70h, Default=09h)

Bit	Description
7-4	Reserved with default "0h"
3-0	Select Interrupt Level ^{Note1} for Environment Controller

8.8.7 APC/PME Event Enable Register (PER) (Index=F0h, Default=00h)

Bit	Description
7	It is set to 1 when VCCH is off. Write 1 to clear this bit. This bit is ineffective if 0 is written to this bit.
6	Reserved
5	Reserved with default "0h"
4	0: PS/2 Mouse event disabled 1: PS/2 Mouse event enabled

Bit	Description
3	0: Keyboard event disabled 1: Keyboard event enabled
2	Reserved
1	Reserved
0	0: CIR event disabled 1: CIR event enabled

8.8.8 APC/PME Status Register (PSR) (Index=F1h, Default=00h)

Bit	Description
7	It is set to 1 when VCC is on at the previous AC power failure and 0 when VCC is off.
6	Reserved
5	Reserved
4	0: No PS/2 Mouse Event Detected 1: PS/2 Mouse Event Detected
3	0: No Keyboard Event Detected 1: Keyboard Event Detected
2	Reserved
1	Reserved
0	0: No CIR event Detected 1: CIR event Detected

8.8.9 APC/PME Control Register 1 (PCR 1) (Index=F2h, Default=00h)

Bit	Description
7	PER and PSR Normal Run Access Enable
6	PME# Output Control 0: Enable 1: Disable
5	This bit is restored automatically to the previous VCC state before the power failure occurs.
4	Disables all APC events after the power failure occurs, excluding PANSWH#.
3	Keyboard event mode selection when VCC is on 1: Determined by PCR 2 0: Pulse falling edge on KCLK
2	Mouse event when VCC is off 1: Click Key twice sequentially 0: Pulse falling edge on MCLK
1	Mouse event when VCC is on 1: Click Key twice sequentially 0: Pulse falling edge on MCLK
0	CIRRX1 Pin Selection 1: Pin 84 0: Pin 85

8.8.10 Environment Controller Special Configuration Register (Index=F3h, Default=00h)

Bit	Description
7-6	Scan Frequency of H/W Monitor 00: 1Hz 01: 2Hz 10: 4Hz 11: 8Hz
5-1	Reserved
0	1: IRQ sharing 0: Normal

8.8.11 APC/PME Control Register 2 (PCR 2) (Index=F4h, Default=00h)

Bit	Description
7	Disable KCLK/KDAT and MCLK/MDAT Auto-swap 0: Enable 1: Disable
6	Reserved
5	PSON# state when VCCH is switched from off to on 0: High-Z (default power OFF) 1: Inverting of PSIN
4	Mask PANSWH# Power-on Event
3-2	Key Number of Keyboard Power-up Event 00: 5 Key string mode, 3 keys simultaneous mode 01: 4 Key string mode, 2 keys simultaneous mode 10: 3 Key string mode, 1 key simultaneous mode 11: 2 Key string mode, Reserved (Not Valid for Simultaneous mode)
1-0	Keyboard Power-up Event Mode Selection 00: KCLK falling edge 01: Key string mode 10: Simultaneous Key Stroke mode 11: Reserved

8.8.12 APC/PME Special Code Index Register (Index=F5h)

Bit	Description
7-6	Reserved (should be "00")
5-0	Indicate which Identification Key Code or CIR code register to be read/written via 0xF6

8.8.13 APC/PME Special Code Data Register (Index=F6h)

There are 5 bytes for the Key String mode, 3 bytes for Stroke Keys at the same time mode and CIR event codes.

8.9 KBC (keyboard) Configuration Registers (LDN=05h)

8.9.1 KBC (keyboard) Activate (Index=30h, Default=01h)

Bit	Description
7-1	Reserved
0	KBC (keyboard) Enable 1: Enable 0: Disable

8.9.2 KBC (keyboard) Data Base Address MSB Register (Index=60h, Default=00h)

Bit	Description
7-4	Read only as "0h" for Base Address [15:12]
3-0	Read/write , mapped as Base Address [11:8]

8.9.3 KBC (keyboard) Data Base Address LSB Register (Index=61h, Default=60h)

Bit	Description
7-0	Read/write , mapped as Base Address[7:0]

8.9.4 KBC (keyboard) Command Base Address MSB Register (Index=62h, Default=00h)

Bit	Description
7-4	Read only as "0h" for Base Address[15:12]
3-0	Read/write , mapped as Base Address[11:8]

8.9.5 KBC (keyboard) Command Base Address LSB Register (Index=63h, Default=64h)

Bit	Description
7-0	Read/write , mapped as Base Address[7:0]

8.9.6 KBC (keyboard) Interrupt Level Select (Index=70h, Default=01h)

Bit	Description
7-4	Reserved with default "0h"
3-0	Select Interrupt Level ^{Note1} for KBC (keyboard)

8.9.7 KBC (keyboard) Interrupt Type (Index=71h, Default=02h)

This register indicates the type of interrupt set for KBC (keyboard) and is **read only** as “02h” when bit 0 of the KBC (keyboard) Special Configuration Register is cleared. When bit 0 is set, this type of interrupt can be selected as level or edge trigger.

Bit	Description
7-2	Reserved
1	1: High level 0: Low level
0	1: Level type 0: Edge type

8.9.8 KBC (keyboard) Special Configuration Register (Index=F0h, Default=08h)

Bit	Description
7-5	Reserved (must be 000b)
4	1: IRQ sharing 0: Normal
3	1: KBC's clock 8 MHz 0: KBC's clock 12 MHz
2	1: Key lock enabled 0: Key lock disabled
1	1: The type of interrupt for KBC (keyboard) can be changed. 0: The type of interrupt for KBC (keyboard) is fixed.
0	Reserved

8.10 KBC (mouse) Configuration Registers (LDN=06h)

8.10.1 KBC (mouse) Activate (Index=30h, Default=00h)

Bit	Description
7-1	Reserved
0	KBC (mouse) Enable 1: Enable 0: Disable

8.10.2 KBC (mouse) Interrupt Level Select (Index=70h, Default=0Ch)

Bit	Description
7-4	Reserved with default "0h"
3-0	Select Interrupt Level ^{Note1} for KBC (mouse)

8.10.3 KBC (mouse) Interrupt Type (Index=71h, Default=02h)

This register indicates the type of interrupt used for KBC (mouse) and is **read only** as "02h" when bit 0 of the KBC (mouse) Special Configuration Register is cleared. When bit 0 is set, the type of interrupt can be selected as level or edge trigger.

Bit	Description
7-2	Reserved
1	1: High level 0: Low level
0	1: Level type 0: Edge type

8.10.4 KBC (mouse) Special Configuration Register (Index=F0h, Default=00h)

Bit	Description
7-2	Reserved with default "00h"
1	1: IRQ sharing 0: Normal
0	1: The type of interrupt for KBC (mouse) can be changed. 0: The type of interrupt for KBC (mouse) is fixed.

8.11 GPIO Configuration Registers (LDN=07h)

8.11.1 SMI# Normal Run Access Base Address MSB Register (Index=60h, Default=00h)

Bit	Description
7-4	Read only as "0h" for Base Address [15:12]
3-0	Read/write , mapped as Base Address [11:8]

8.11.2 SMI# Normal Run Access Base Address LSB Register (Index=61h, Default=00h)

Bit	Description
7-2	Read/write , mapped as Base Address [7:2]
1-0	Read only as "00b"

8.11.3 Simple I/O Base Address MSB Register (Index=62h, Default=00h)

Bit	Description
7-4	Read only as "0h" for Base Address [15:12]
3-0	Read/write , mapped as Base Address [11:8]

8.11.4 Simple I/O Base Address LSB Register (Index=63h, Default=00h)

Bit	Description
7-0	Read/write , mapped as Base Address[7:0]

8.11.5 Serial Flash I/F Base Address MSB Register (Index=64h, Default=00h)

Bit	Description
7-4	Read only as "0h" for Base Address [15:12]
3-0	Read/write , mapped as Base Address [11:8]

8.11.6 Serial Flash I/F Base Address LSB Register (Index=65h, Default=00h)

Bit	Description
7-3	Read/write , mapped as Base Address [7:3]
2-0	Read only as "000b"

8.11.7 Panel Button De-bounce Interrupt Level Select Register (Index=70h, Default=00h)

Bit	Description
7-4	Reserved
3-0	Select Interrupt level ^{Note1} for Panel Button De-bounce

8.11.8 Watch Dog Timer Control Register (Index=71h, Default=00h)

Bit	Description
7	WDT is reset upon a CIR interrupt.
6	WDT is reset upon a KBC (mouse) interrupt.
5	WDT is reset upon a KBC (keyboard) interrupt.
4	Reserved
3-2	Reserved
1	Force Time-out This bit is self-clearing.
0	WDT Status 1: WDT value is equal to 0. 0: WDT value is not is equal to 0.

8.11.9 Watch Dog Timer Configuration Register (Index=72h, Default=001s0000b)

Bit	Description
7	WDT Time-out Value Select 1 1: Second 0: Minute
6	WDT Output through KRST (pulse) Enable 1: Enable 0: Disable
5	WDT Time-out Value Extra Select 1: 64ms x WDT Timer-out value (default = 4s) 0: Determined by WDT Time-out value select 1 (bit 7 of this register)
4	WDT Output through PWROK1/PWROK2 (pulse) Enable 1: Enable 0: Disable <i>During LRESET#, this bit is select by JP5 power-on strapping option.</i>
3-0	Select Interrupt Level^{Note} for WDT

8.11.10 Watch Dog Timer Time-Out Value (LSB) Register (Index=73h, Default=38h)

Bit	Description
7-0	WDT Time-out Value 7-0

8.11.11 Watch Dog Timer Time-Out Value (MSB) Register (Index=74h, Default=00h)

Bit	Description
7-0	WDT Time-out Value 15-8

8.11.12 GPIO Pin Set 1, 2, 3, 4, 5, 6 ,7 and 8 Polarity Registers (Index=B0h, B1h, B2h, B3h and B4h, Default=00h)

These registers are used to program the GPIO pin type for polarity inverting or non-inverting.

Bit	Description
7-0	1: Inverting 0: Non-inverting

8.11.13 GPIO Pin Set 1, 3, 4, 5 and 6 Pin Internal Pull-up Enable Registers (Index=B8h, BAh, BBh, BCh and BDh, Default=00h)

These registers are used to enable the GPIO pin internal pull-up. (There are no internal P/U function for GP20~GP27, GP56, GP57, GP60, GP61, GP62.)

Bit	Description
7-0	1: Enable 0: Disable

8.11.14 Simple I/O Set 1, 2, 3, 4 and 5 Enable Registers (Index=C0h, C1h, C2h, C3h and C4h, Default=01h, 00h, 00h, 40h, 00h and 00h)

These registers are used to select the function as the Simple I/O function or the Alternate function.

Bit	Description
7-0	1: Simple I/O function 0: Alternate function

8.11.15 Simple I/O Set 1, 2, 3, 4, 5, 6, 7 and 8 Output Enable Registers (Index=C8h, C9h, CAh, CBh, CCh, CDh, CEh and CFh, Default=01h, 00h, 00h, 40h, 00h and 00h)

These registers are used to determine the direction of the Simple I/O.

Bit	Description
7-0	0: Input mode 1: Output mode

8.11.16 Panel Button De-bounce 0 Input Pin Mapping Registers (Index=E0h, Default=00h)

Bit	Description
7	Reserved
6	IRQ Enable
5-0	Input Pin Location Please see note4, the location mapping table.

8.11.17 Panel Button De-bounce 1 Input Pin Mapping Registers (Index=E1h, Default=00h)

Bit	Description
7-6	Reserved
5-0	Input Pin Location Please see note4, the location mapping table.

8.11.18 IRQ External Routing 1-0 Input Pin Mapping Registers (Index=E3h-E2h, Default=00h)

Bit	Description
7	Reserved
6	IRQ Enable
5-0	Input Pin Location Please see note4, the location mapping table.

8.11.19 IRQ External Routing 1-0 Interrupt Level Selection Register (Index=E4h, Default=00h)

Bit	Description
7-4	Select Interrupt level ^{Note1} for IRQ External Routing 1
3-0	Select Interrupt level ^{Note1} for IRQ External Routing 0

8.11.20 VID Watchdog timer 0 Value Register (Index=E5h, Default=00h)

Bit	Description
7-0	VID Watchdog Timer 0 Value Writing to this register will load a new counter. Reading it when VID Watchdog is disabled (bit2 of Index FFh = 0) will respond the setting value. Reading it when VID Watchdog is enabled (bit 2 of Index FFh = 1) will respond the left counters to timeout.

8.11.21 VID Watchdog timer 1 Value Register (Index=E6h, Default=00h)

Bit	Description
7-0	VID Watchdog Timer 1 Value Writing to this register will load a new counter. Reading it when VID Watchdog is disabled (bit3 of Index FFh = 0) will respond the setting value. Reading it when VID Watchdog is enabled (bit3 of Index FFh = 1) will respond the left counters to timeout.

8.11.22 VID Detecting Value Register (Index=E8h, Default=00h)

Bit	Description
7-0	VID Detecting Value [7:0] When VID inputs a value, it will be switched to the dynamic mode automatically.

8.11.23 Bus Select Control Register (Index=E9h, Default=07h)

Bit	Description
7-6	Reset Selection 00: RSMRST#. 01: LRESET#. 10: POWEROK 11: Reserved
5	Bus Select function Disable 0: Enable 1: Disable

Bit	Description
4	Bus Select Output Enable 0: Transparent mode 1: Enable registers output
3	Bit[2:0] Reading select This bit will select the reading of bit[2:0]. 0: Bus Select Input [2:0] 1: Bus Select Output Register values
2-0	Bus Select Input/Output [2:0] These three bits are bus select Input/output register. When reading, they will report the status of the bus select input if bit 3 = 0 or the values of the bus select output registers if bit 3 = 1. The values of bus select output registers will not be shown on the bus select output pins unless bit 4 = 1.

8.11.24 SMI# Control Register 1 (Index=F0h, Default=00h)

Bit	Description
7	Reserved
6	Enables the generation of an SMI# due to KBC (Mouse)'s IRQ (EN_MIRQ)
5	Enables the generation of an SMI# due to KBC (Keyboard)'s IRQ (EN_KIRQ)
4	Enables the generation of an SMI# due to Environment Controller's IRQ (EN_ECIRQ)
3	Enables the generation of an SMI# due to Parallel Port's IRQ (EN_PIRQ)
2	Enables the generation of an SMI# due to Serial Port 2's IRQ (EN_S2IRQ)
1	Enables the generation of an SMI# due to Serial Port 1's IRQ (EN_S1IRQ)
0	Enables the generation of an SMI# due to FDC's IRQ (EN_FIRQ)

8.11.25 SMI# Control Register 2 (Index=F1h, Default=00h)

Bit	Description
7	Forces to clear all the SMI# status register bits, non-sticky
6	0: Edge trigger 1: Level trigger
5-4	Reserved
3	Reserved
2	Enables the generation of an SMI# due to WDT's IRQ (EN_WDT)
1	Enables the generation of an SMI# due to CIR's IRQ (EN_CIR)
0	Enables the generation of an SMI# due to PBD's IRQ (EN_PBD)

8.11.26 SMI# Status Register 1 (Index=F2h, Default=00h)

This register is used to read the status of SMI# inputs.

Bit	Description
7	Reserved
6	KBC (PS/2 Mouse)'s IRQ
5	KBC (Keyboard)'s IRQ
4	Environment Controller's IRQ
3	Parallel Port's IRQ
2	Serial Port 2's IRQ
1	Serial Port 1's IRQ
0	FDC's IRQ

8.11.27 SMI# Status Register 2 (Index=F3h, Default=00h)

This register is used to read the status of SMI# inputs.

Bit	Description
7-6	Panel Button De-bounce Status 1-0 Writing 1 will reset the status. 0: None detected. 1: Detected.
5-4	Reserved
3	Reserved
2	WDT's IRQ
1	CIR's IRQ
0	PBD's IRQ

8.11.28 SMI# Pin Mapping Register (Index=F4h, Default=00h)

Bit	Description
7-6	Reserved
5-0	SMI# Pin Location Please see note 4, the location mapping table.

8.11.29 Hardware Monitor Thermal Output Pin Mapping Register (Index=F5h, Default=00h)

Bit	Description
7-6	Reserved
5-0	Thermal Output Pin Location Please see note 4, the location mapping table.

8.11.30 Hardware Monitor Alert Beep Pin Mapping Register (Index=F6h, Default=00h)

Bit	Description
7-6	Reserved
5-0	Alert Beep Pin Location Please see note 4, the location mapping table.

8.11.31 Keyboard Lock Pin Mapping Register (Index=F7h, Default=00h)

Bit	Description
7-6	Reserved
5-0	Keyboard Lock Pin Location Please see note 4, the location mapping table.

8.11.32 GP LED Blinking 1 Pin Mapping Register (Index=F8h, Default=00h)

Bit	Description
7-6	Reserved
5-0	GP LED Blinking 1 Location Please see note 4, the location mapping table.

8.11.33 GP LED Blinking 1 Control Register (Index=F9h, Default=00h)

Bit	Description
7-4	Reserved
3	GP LED Blinking 1 Short Low Pulse Enable
2-1	GP LED 1 Frequency Control 00: 4 Hz 01: 1 Hz 10: 1/4 Hz 11: 1/8 Hz
0	GP LED Blinking 1 Output Low Enable

8.11.34 GP LED Blinking 2 Pin Mapping Register (Index=FAh, Default=00h)

Bit	Description
7-6	Reserved
5-0	GP LED Blinking 2 Location Please see note 4, the location mapping table.

8.11.35 GP LED Blinking 2 Control Register (Index=FBh, Default=00h)

Bit	Description
7-4	Reserved
3	GP LED Blinking 2 Short Low Pulse Enable
2-1	GP LED 2 Frequency Control 00: 4 Hz 01: 1 Hz 10: 1/4 Hz 11: 1/8 Hz
0	GP LED Blinking 2 Output Low Enable

8.11.36 VID Input Register (Index=FCh, Default=--h)

Bit	Description
7-0	VID 7-0 Input These inputs are read-only. Writing "1" to bit 0 to update the initial VID input.

8.11.37 VID Output/Programed Output Register (Index=FDh, Default=00h)

Bit	Description
7-0	VID 7-0 Output or Programed Output Value If DYNAMIC_en is low, this register is VID Output value for software mode. If the bit is high, this register is the Programed output values. In the dynamic VID mode, the programmed output value is 2's complement. For example, when the 6-bit table is selected, only bit 5-0 are valid. 000011b means 3 steps higher than inputs, and 111011b means 5 steps lower than inputs.

8.11.38 VID Watchdog Timer Control Register (Index=FEh, Default=00h)

Bit	Description
7-6	VID_READING_SEL. VID 7-0 Reading Selection 00: Bit 7-0 is the initial value of VID input. 01: Bit 7-0 is the current value of VID input. 10: Bit 7-0 is the current value of VID output. 11: Reserved
5-4	Reserved
3-2	Dynamic Table Selection 00: VRM9 01: VRM10 (6-bit VID) 10: VRM11 (7-bit VID) 11: VRM11 (8-bit VID)
1	DYNAMIC_en. VID Output Selection 1: Dynamic VID output The value of VIDOUT output pins is generated from the input signals VIDIN and VID 7-0 output values (bit7-0). If VID input and output are the same pin, this bit cannot be enabled. 0: Software The value of VIDOUT output pins is directly VID 7-0 output values (bit7-0).
0	VID_OE. VID Output Enable 1: Output 0: Input

8.11.39 VID Watchdog timer Control Register (Index=FFh, Default=00h)

Bit	Description
7	VID Automatic Switch to Dynamic Mode 1: Enable 0: Disable
6	Reserved
5	VID Watchdog 1 Time-unit 1: VID watchdog 1 time-unit is 1ms(1/1024). 0: VID watchdog 1 time-unit is 62.5ms(1/16).
4	VID Watchdog 0 Time-unit 1: VID watchdog 0 time-unit is 1ms(1/1024). 0: VID watchdog 0 time-unit is 62.5ms(1/16).
3	VID Watchdog 1 Enable 1: Enable VID watchdog timer 1. 0: Disable VID watchdog timer 1.
2	VID Watchdog 0 Enable 1: Enable VID watchdog timer 0. 0: Disable VID watchdog timer 0.
1	VID Watchdog 1 Time-out 1: VID watchdog 1 timeout occurs. Writing 1 to it will clear itself. 0: No VID watchdog 1 timeout event
0	VID Watchdog 0 Time-out 1: VID watchdog 0 timeout occurs. Writing 1 to it will clear itself. 0: No VID watchdog 0 timeout event.

8.12 Consumer IR Configuration Registers (LDN=0Ah)

8.12.1 Consumer IR Activate (Index=30h, Default=00h)

Bit	Description
7-1	Reserved
0	Consumer IR Enable 1: Enable 0: Disable

8.12.2 Consumer IR Base Address MSB Register (Index=60h, Default=03h)

Bit	Description
7-4	Read only with "0h" for Base Address[15:12]
3-0	Read/write , mapped as Base Address[11:8]

8.12.3 Consumer IR Base Address LSB Register (Index=61h, Default=10h)

Bit	Description
7-3	Read/write , mapped as Base Address[7:3]
2-0	Read only as "000b"

8.12.4 Consumer IR Interrupt Level Select (Index=70h, Default=0Bh)

Bit	Description
7-4	Reserved with default "0h"
3-0	Select the interrupt level Note1 for Consumer IR

8.12.5 Consumer IR Special Configuration Register (Index=F0h, Default=00h)

Bit	Description
7-1	Reserved with default "00h"
0	1: IRQ sharing 0: Normal

Note 1:

Interrupt level mapping

Fh-Dh: not valid

Ch: IRQ12

3h: IRQ3

2h: not valid

1h: IRQ1

0h: no interrupt selected

Note 2:

DMA channel mapping

7h-5h: not valid

4h: no DMA channel selected

3h: DMA3

2h: DMA2

1h: DMA1

0h: DMA0

Note 3:

Except the standard mode, COM1 and COM2 cannot be selected in the same mode.

Note 4: The location mapping table

Location	Description
001 000	GP10 (pin 84). Powered by VCCH.
001 001	GP11 (pin 34).
001 010	GP12 (pin 33).
001 011	GP13 (pin 32).
001 100	GP14 (pin 31).
001 101	GP15 (pin 3).
001 110	GP16 (pin 2).
001 111	GP17 (pin 28).
010 000	GP20 (pin 27). Powered by VCCH.
010 001	GP21 (pin 26). Powered by VCCH.
010 010	GP22 (pin 25). Powered by VCCH.
010 011	GP23 (pin 24). Powered by VCCH.
010 100	GP24 (pin 23). Powered by VCCH.
010 101	GP25 (pin 22). Powered by VCCH.
010 110	GP26 (pin 21). Powered by VCCH.
010 111	GP27 (pin 20). Powered by VCCH.
011 000	GP30 (pin 19).
011 001	GP31 (pin 18).
011 010	GP32 (pin 17).
011 011	GP33 (pin 16).
011 100	GP34 (pin 14).
011 101	GP35 (pin 13).
011 110	GP36 (pin 12).
011 111	GP37 (pin 11).
100 000	GP40 (pin 79). Powered by VCCH.
100 001	GP41 (pin 78). Powered by VCCH.
100 010	GP42 (pin 76). Powered by VCCH.
100 011	GP43 (pin 75). Powered by VCCH.
100 100	GP44 (pin 72). Powered by VCCH.
100 110	GP46 (pin 70). Powered by VCCH.
100 111	GP47 (pin 66).
101 000	GP50 (pin 48).
101 001	GP51 (pin 10).
101 010	GP52 (pin 9).
101 011	GP53 (pin 77). Powered by VCCH.
101 100	GP54 (pin 73). Powered by VCCH.
101 101	GP55 (pin 85). Powered by VCCH.
101 110	GP56 (pin 83). Powered by VCCH.
101 111	GP57 (pin 82). Powered by VCCH.
Else	Reserved

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9. Functional Description

9.1 LPC Interface

The IT8720F supports the peripheral side of the LPC I/F as described in the LPC Interface Specification Rev.1.0 (Sept. 29, 1997). In addition to the required signals (LAD3-0, LFRAME#, LRESET#, LCLK (LCLK is the same as PCICLK.)), the IT8720F also supports LDRQ#, SERIRQ and PME#.

9.1.1 LPC Transactions

The IT8720F supports the necessary transfer cycle types described in the LPC I/F specification. Memory read and Memory write cycles are used for the Flash I/F. I/O read and I/O write cycles are used for the programmed I/O cycles. DMA read and DMA write cycles are used for DMA cycles. All of these cycles are characteristic of the single byte transfer.

For LPC host I/O read or write transactions, the Super I/O module processes a positive decoding, and the LPC interface can respond to the result of the current transaction by sending out SYNC values on LAD[3:0] signals or leave LAD[3:0] tri-state depending on its result.

For DMA read or write transactions, the LPC interface will react according to the DMA requests from the DMA devices in the Super I/O modules, and decide whether to ignore the current transaction or not.

The FDC and ECP are 8-bit DMA devices, so if the LPC Host initializes a DMA transaction with data size of 16/32 bits, the LPC interface will process the first 8-bit data and respond with an SYNC ready (0000b) which will terminate the DMA burst. The LPC interface will then re-issue another LDRQ# message to assert DREQn after finishing the current DMA transaction.

9.1.2 LDRQ# Encoding

The Super I/O module provides two DMA devices: the FDC and the ECP. The LPC Interface provides LDRQ# encoding to reflect the DREQ[3:0] status. Two LDRQ# messages or different DMA channels may be issued back-to-back to trace DMA requests quickly. But, four PCI clocks will be inserted between two LDRQ# messages of the same DMA channel to guarantee that there are at least 10 PCI clocks for one DMA request to change its status. (The LPC host will decode these LDRQ# messages, and send those decoded DREQn to the legacy DMA controller which runs at 4 MHz or 33/8 MHz).

9.2 Serialized IRQ

The IT8720F follows the specification of Serialized IRQ Support for PCI System, Rev. 6.0, September 1, 1995, to support the serialized IRQ feature, and is able to interface most PC chipsets. The IT8720F encodes the parallel interrupts to an SERIRQ which will be decoded by the chipset with built-in Interrupt Controllers (two 8259 compatible modules).

9.2.1 Continuous Mode

When in the Continuous mode, the SIRQ host initiates the Start frame of each SERIRQ sequence after sending out the Stop frame by itself. (The next Start frame may or may not begin immediately after the turnaround state of the current Stop frame.) The SERIRQ is always activated and SIRQ host keeps polling all the IRQn and system events, even though no IRQn status is changed. The SERIRQ enters the Continuous mode following a system reset.

9.2.2 Quiet Mode

In the Quiet mode, when the situation that one SIRQ Slave detects its input IRQn/events have been changed, it may initiate the first clock of Start frame. The SIRQ host can then follow to complete the SERIRQ sequence.

In the Quiet mode, the SERIRQ has no activity following the Stop frame until it is initiated by SIRQ Slave, which implies low activity = low mode power consumption.

9.2.3 Waveform Samples of SERIRQ Sequence

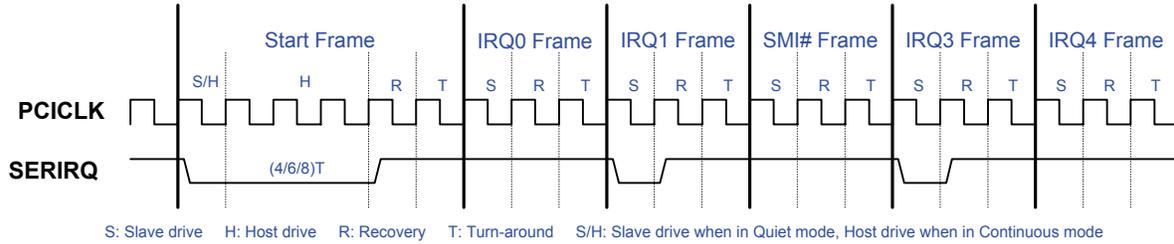


Figure 9-1. Start Frame Timing

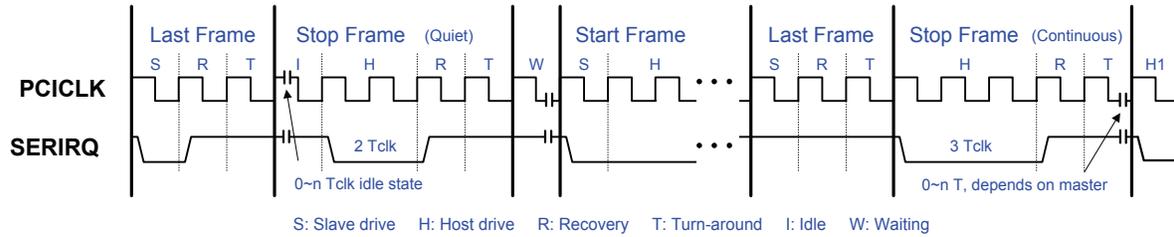


Figure 9-2. Stop Frame Timing

9.2.4 SERIRQ Sampling Slot

Slot Number	IRQn/ Events	#of Clocks Past Start	IT8720F
1	IRQ0	2	-
2	IRQ1	5	Y
3	SMI#	8	Y
4	IRQ3	11	Y
5	IRQ4	14	Y
6	IRQ5	17	Y
7	IRQ6	20	Y
8	IRQ7	23	Y
9	IRQ8	26	Y
10	IRQ9	29	Y
11	IRQ10	32	Y
12	IRQ11	35	Y
13	IRQ12	38	Y
14	IRQ13	41	-
15	IRQ14	44	Y
16	IRQ15	47	Y
17	IOCHCK#	50	-
18	INTA#	53	-
19	INTB#	56	-
20	INTC#	59	-
21	INTD#	62	-
32:22	Unassigned	95 / 65	-

9.3 General Purpose I/O

The IT8720F provides eight sets of flexible I/O control and special functions for the system designers via a set of multi-functional General Purpose I/O pins (GPIO). The GPIO functions will not be performed unless the related enable bits of the GPIO Multi-function Pin Selection registers (Index 25h, 26h, 27h, 28h and 29h of the Global Configuration Registers) are set. The GPIO functions include the simple I/O function and alternate function, and the function selection is determined by the Simple I/O Enable Registers (LDN=07h, Index=C0h, C1h, C2h, C3h and C4h).

The Simple I/O function includes a set of registers, which correspond to the GPIO pins. All control bits are divided into eight registers. The accessed I/O ports are programmable and are five consecutive I/O ports (Base Address+0, Base Address+1, Base Address+2, Base Address+3, Base Address+4, Base Address+5, Base Address+6, Base Address+7). Base Address is programmed on the registers of GPIO Simple I/O Base Address LSB and MSB registers (LDN=07h, Index=60h and 61h).

The Alternate Function provides several special functions for users, including Watch Dog Timer, SMI# output routing, External Interrupt routing, Panel Button De-bounce, Keyboard Lock input routing, LED Blinking, Thermal output routing, and Beep output routing. The last two are sub-functions of the Hardware Monitor. (GPIO set 6, 7, 8 only support the simple I/O function.)

The Panel Button De-bounce is an input function. After the panel button de-bounce is enabled, a related status bit will be set when an active low pulse is detected on the GPIO pin. The status bits will be cleared by writing 1's to them. Panel Button De-bounce Interrupt will be issued if any one of the status bit is set. However, the new setting status will not issue another interrupt unless the previous status bit is cleared before being set.

The Key Lock function locks the keyboard to inhibit the keyboard interface. The programming method is to set bit 2 on the register Index F0h of KBC (keyboard) (LDN=5). The pin location mapping, Index F7h must also be programmed correctly.

The Blinking function provides a low frequency blink output. By connecting it to some external components, it can be used to control a power LED. There are several frequencies that can be selected.

The Watch Dog Timer (WDT) function is constituted by a time counter, a time-out status register, and the timer reset control logic. The time-out status bit may be mapped to an interrupt or KRST# through the WDT Configuration register. The WDT has a programmable time-out range from 1 to 65535 minutes or 1 to 65535 seconds. The units are also programmable, either a minute or a second, via bit7 of the WDT Configuration register. When the WDT Time-out Value register is set to a non-zero value, the WDT loads the value and begin counting down from the value. When the value reaches to 0, the WDT status register will be set. There are many system events that can reload the non-zero value into the WDT. They include a CIR interrupt, a Keyboard Interrupt, a Mouse Interrupt. The effect on the WDT for each of the events may be enabled or disabled through bits in the WDT control register. No matter what the value in the time counter is, the host may force a time-out to occur by writing a "1" to bit 1 of the WDT Configuration register.

The External Interrupt routing function provides a useful feature for motherboard designers. Through this function, the parallel interrupts of other on-board devices can be easily re-routed into the Serial IRQ.

The SMI# is a non-maskable interrupt dedicated to the transparent power management. It consists of different enabled interrupts generated from each of the functional blocks in the IT8720F. The interrupts are redirected as the SMI# output via the SMI# Control Register 1 and SMI# Control Register 2. The SMI# Status Registers 1 and 2 are used to read the status of the SMI input events. All the SMI# Status Register bits can be cleared when the corresponding source events become invalidated. These bits can also be cleared by writing 1 to bit 7 of SMI# Control Register 2 no matter whether the events of the corresponding sources are invalidated or not. The SMI# events can be programmed as the pulse mode or level mode whenever an SMI# event occurs. The logic equation of the SMI# event is described below:

SMI# event = (EN_FIRQ and FIRQ) or (EN_S1IRQ and S1IRQ) or (EN_S2IRQ and S2IRQ) or (EN_PIRQ and PIRQ) or (EN_EC and EC_SMI) or (EN_PBDIRQ or PBDIRQ) or (EN_KIRQ and KIRQ) or (EN_MIRQ and MIRQ) or (EN_CIR and CIR_IRQ) or (EN_WDT and WDT_IRQ)

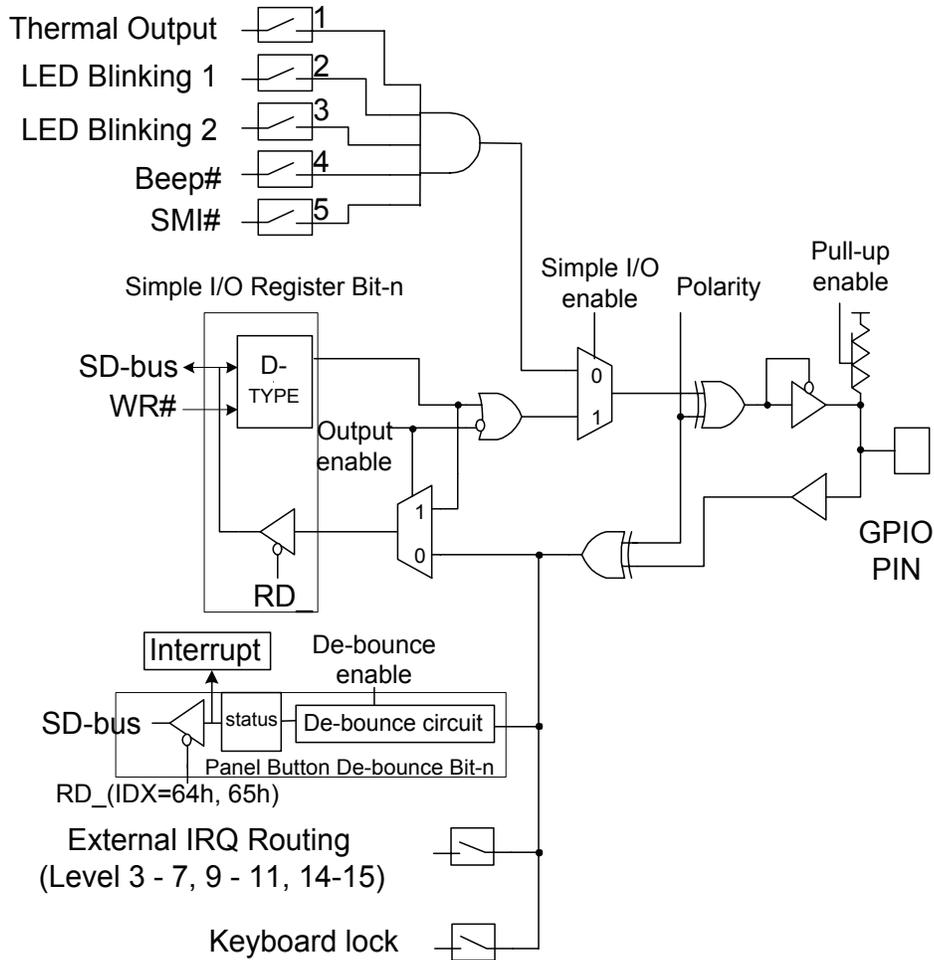


Figure 9-3. General Logic of GPIO Function

9.4 Advanced Power Supply Control and Power Management Event (PME#)

The circuit for advanced power supply control (APC) provides three power-up events, Keyboard, Mouse and CIR. When any of these three events is activated, PWRON# will perform a low state until VCC is switched to the ON state. The three events include the followings:

1. Detection of KCLK edge or special pattern of KCLK and KDAT. The special pattern of KCLK means pressing pre-set key string sequentially, and KDAT means pressing pre-set keys simultaneously.
2. Detection of MCLK edge or special pattern of MCLK and MDAT. The special pattern of MCLK and MDAT means clicking on any mouse button twice sequentially.
3. Receiving CIR patterns match the previously stored pattern stored at the APC/PME Special Code Index and Data Register.

The PANSWH# and PSON# are especially designed for the system. PANSWH# serves as a main power switch input, which is wire-AND to the APC output PWRON#. PSON# is the ATX Power control output, which is a power-failure gating circuit. The power-failure gating circuit is responsible for gating the PSIN input until PANSWH# becomes active when the VCCH is switched from OFF to ON.

The power-failure gating circuit can be disabled by setting the APC/PME Control Register 2 (LDN=04h, index F4h, bit 5). The gating circuit also provides an auto-restore function. When the bit 5 of PCR1 is set, the previous PSON# state will be restored when the VCCH is switched from OFF to ON.

The Mask PWRON# Activation bit (bit 4 of PCR 1) is used to mask all Power-up events except Switch on event when the VCCH state is just switched from FAIL to OFF. In other words, when this bit is set and the power state is switched from FAIL to OFF, the only validated function is PANSWH#.

The PCR2 register is responsible for determining the Keyboard power up events and APC conditions. Bit 4 is used to mask the PANSWH# power-on event on the PWRON# pin. To enable this bit, the keyboard power-up event should be enabled and set by (1) pressing pre-set key string sequentially or (2) stroking pre-set keys simultaneously. The APC/PME# special code index and data registers are used to specify the special key codes in the special power-up events of (1) pressing pre-set key string sequentially or (2) stroking pre-set keys simultaneously.

A CIR event is generated if the input CIR RX pattern is the same as the previously stored pattern stored at PME Special Code Index and Data Registers (LDN=04h, Index=F5h and F6h). The total maximum physical codes are nineteen bytes (from Index 20h to 32h). The first byte (Index 20h) is used to specify the pattern length (in bytes). Bits [7:4] are used when VCC is on; and Bits [3:0] when VCC goes OFF. The length represented in each 4 bits will be incremented by 3 internally as the actual length is to be compared. For most of the CIR protocols, the first several bytes are always the same for each key (or pattern). The differences are always placed in the last several bytes. Thus, the system designer can program the IT8720F to generate a CIR PME# event as any keys when VCC is ON and a special key (i.e. POWER-ON) when VCC is OFF.

All APC registers (Index=F0h, F2h, F4h, F5h and F6h) are powered by back-up power (VBAT) when VCCH is OFF.

PME# is used to wake up the system from low-power states (S1-S5). There will be five events of APC's to generate PME#. A falling edge on these pins issues PME# events if the enable bits are set.

9.5 SPI Serial Flash Controller

9.5.1 Overview

The SPI Serial Flash Controller is an LPC to the serial Flash I/F controller.

9.5.2 Features

- SPI Interface
- LPC memory cycle and firmware memory cycle supported

9.5.3 Register Descriptions

Table 9-1. Memory Stick Register List

Address	R/W	Default	Name
Base + 0h	R/W	20h	Control Register (SPI_CTRL)
Base + 1h	R/W	00h	Command Register (SPI_CMD)
Base + 2h	R/W	00h	Address 0 Register (SPI_ADDR0)
Base + 3h	R/W	00h	Address 1 Register (SPI_ADDR1)
Base + 4h	R/W	00h	Address 2 Register (SPI_ADDR2)
Base + 5h	R	--	Input Data 0 Register (SPI_IDATA0)
Base + 6h	R	--	Input Data 1 Register (SPI_IDATA1)
Base + 7h	R/W-R	00h/--	Output Data Register (SPI_ODATA)/ Input Data 2 Register (SPI_IDATA2)

9.5.3.1 Control Register (SPI_CTRL)

Address: Base address + 0h

Bit	R/W	Default	Description
7	R	-	SPI Status Report SPI I/F status 0: SPI I/F is idle 1: SPI I/F is busy
6	R/W	0b	Start IO Transfer Start SPI cycle with the instruction/parameter given through I/O port. 0: No Start IO 1: Enable Start IO
5	R/W	1b	Multiple Byte Mode Enable Multiple Byte mode in LPC memory write/read cycle. 0: Disable 1: Enable
4	R/W	0b	SCK Selection Select the SCK frequency. 0: 33MHz/2 1: 33MHz

Bit	R/W	Default	Description
3-2	R/W	00b	Input Data Byte These bits determine the number of input data byte in the Start IO mode. 00: None 01: 1 byte (SPI_DATAI0) 10: 2 bytes (SPI_DATAI0, SPI_DATAI1) 11: 3 bytes (SPI_DATAI0, SPI_DATAI1, SPI_DATAI2)
1-0	R/W	00b	Output Data Byte These bits determine the number of the output data byte (including Instruction, Address, Data) in the Start IO mode. 00: 1 byte (SPI_CMD) 01: 2 bytes (SPI_CMD, SPI_DATAO) 10: 4 bytes (SPI_CMD, ADDR2, ADDR1, ADDR0) 11: 5 bytes (SPI_CMD, ADDR2, ADDR1, ADDR0, SPI_DATAO)

9.5.3.2 Command Register (SPI_CMD)

Address: Base address + 1h

Bit	R/W	Default	Description
7-0	R/W	00h	Command Register (SPI_CMD [7:0]) This register will set the Instruction command code in the Start IO mode. (The first byte)

9.5.3.3 Address 0 Register (SPI_ADDR0)

Address: Base address + 2h

Bit	R/W	Default	Description
7-0	R/W	00h	Address 0 Register (SPI_ADDR0 [7:0]) This register will set the Address [7:0] in the Start IO mode.

9.5.3.4 Address 1 Register (SPI_ADDR1)

Address: Base address + 3h

Bit	R/W	Default	Description
7-0	R/W	00h	Address 1 Register (SPI_ADDR1 [7:0]) This register will set the Address [15:8] in the Start IO mode.

9.5.3.5 Address 2 Register (SPI_ADDR2)

Address: Base address + 4h

Bit	R/W	Default	Description
7-0	R/W	00h	Address 2 Register (SPI_ADDR2 [7:0]) This register will set the Address [23:16] in the Start IO mode.

9.5.3.6 Input Data 0 Register (SPI_IDATA0)

Address: Base address + 5h

Bit	R/W	Default	Description
7-0	R	-	Input Data 0 Register (SPI_IDATA0 [7:0]) This register will set the Input Data 0 byte in the Start IO mode.

9.5.3.7 Input Data 1 Register (SPI_IDATA1)

Address: Base address + 6h

Bit	R/W	Default	Description
7-0	R	-	Input Data 1 Register (SPI_IDATA1 [7:0]) This register will set the Input Data 1 byte in the Start IO mode.

9.5.3.8 Output Data/Input Data 2 Register (SPI_ODATA/ SPI_IDATA2)

Address: Base address + 7h

Bit	R/W	Default	Description
7-0	R/W	00h	Output Data Register (SPI_ODATA [7:0])/ Input Data 2 Register (SPI_IDATA1 [7:0]) This register will set the Output Data byte in the Start IO mode, or Input Data 2 when the number of the input data byte is 3.

9.5.4 Function Descriptions

Programming sequence: All the instruction code and byte numbers should refer to the Serial Flash product specification.

Start IO mode:

```
// 1: Check SPI I/F
IOR [SPI_CTRL];           // check bit7 SPI status

// 2: Set the parameters in any order of write sequence.
IOW [SPI_CMD]    XXh:    // Set SPI Instruction
IOW [SPI_ADDR0] XXh:    // Set SPI Address0, if necessary
IOW [SPI_ADDR1] XXh:    // Set SPI Address1, if necessary
IOW [SPI_ADDR2] XXh:    // Set SPI Address2, if necessary
IOW [SPI_ODATA] XXh:    // Set SPI Output Data, if necessary

// 3: Start SPI I/F
IOW [SPI_CTRL]    {4'h1, Input_data_byte, Output_data_byte};
```

LPC memory cycle:

When the host issues an LPC memory read cycle with the matching memory space, the controller will issue a corresponding SPI read cycle automatically. The controller will pre-read from 0 to 3 byte(s) of data into the read buffers. The number of pre-read data byte(s) is determined by the starting address 0 and 1. The number of bytes will be 3 bytes if the two addresses are 00b. The number will be 2 bytes if the two addresses are 01b. The number will be 1 byte if the two addresses are 10b. There is no pre-read data if the two addresses are 11b. If the address of the next coming LPC memory cycles matches the buffers' address; no SPI read cycle would be issued.

For most types of serial flash products, the Write-Enable instruction through the Start IO mode should be given before issuing the LPC memory write cycle. Normally, each LPC memory cycle will issue a one byte SPI programming cycle (Instruction, Addresses, 1 Data byte). If the Multiple Byte mode is enabled, a multi-byte SPI programming cycle will be issued. For example:

```
// LPC Memory Write Multiple byte mode
// 1: Write-Enable command
IOR [SPI_CTRL];           // check bit7 SPI status
IOW [SPI_CMD]    06h:    // Set SPI Instruction
```

```

IOW [SPI_CTRL]      {4'h3, 2'b00, 2'b00};
                    // Start IO SPI cycle and enable the LPC memory Multiple Byte mode

// 2:  LPC memory write cycles: The first LPC memory cycle will start an SPI cycle and determine the
//      Programming page address. The following LPC memory write cycles must be contiguous
//      addresses.
// And, the total bytes cannot exceed 256 – [starting address 7-0]. These conditions should be
// confirmed by the programmer. The controller will not check them. During this period, the SPI cycle
// will not be finished. Between the two MEMW cycles, the HOLD# pin will be asserted and SCK will be
// forced low.
MEMW  [Starting address]:      // Set SPI Address and the first byte data.
MEMW  [Starting address+1]:    // Set SPI second byte data.
MEMW  [Starting address+2]:    // Set SPI third byte data.
      :
MEMW  [Starting address+N]:    // Set SPI Nth byte data.

// 3:  Terminate SPI I/F
IOW [SPI_CTRL]      {4'h0, 2'b00, 2'b00};
                    // Terminate LPC memory write Page Program mode and SPI cycle

// LPC Memory Read Multiple byte mode
// 1:  Write-Enable command
IOW [SPI_CTRL]      {4'h2, 2'b00, 2'b00};
                    // Enable LPC memory Multiple Byte mode

// 2:  LPC memory read cycles: The first LPC memory cycle will start the SPI cycle and determine the
//      reading address. The following LPC memory read cycles should be the contiguous addresses.
// And, the total bytes will not be limited. The programmer should confirm these conditions.
// The controller will not check them. During this period, the SPI cycle will not be finished. Between the
// two // MEMR cycles, the HOLD# pin will be asserted and SCK will be forced low.
MEMR  [Starting address]:      // Set SPI Address and the first byte data.
MEMR  [Starting address+1]:    // Set SPI second byte data.
MEMR  [Starting address+2]:    // Set SPI third byte data.
      :
MEMR  [Starting address+N]:    // Set SPI Nth byte data.

// 3:  Terminate SPI I/F
IOW [SPI_CTRL]      {4'h0, 2'b00, 2'b00};
                    // Terminate LPC memory Read Multiple Byte mode and SPI cycle

```

9.6 Environment Controller

The Environment Controller (EC), built in the IT8720F, includes seven voltage inputs, three temperature sensor inputs, five FAN Tachometer inputs, and five sets of advanced FAN Controllers. The EC monitors the hardware environment and implements the environmental control for personal computers.

The IT8720F contains an 8-bit ADC (Analog-to-Digital Converter), which is responsible for monitoring the voltages and temperatures. The ADC converts the analog inputs ranging from 0V to 4.096V to 8-bit digital bytes. With additional external components, the analog inputs can be made to monitor different voltage ranges, in addition to monitoring the fixed input range of 0V to 4.096V. Through external thermistors or thermal diodes, the temperature sensor inputs can be converted to 8-bit digital bytes, enabling the sensor inputs to monitor the temperature of various components. A built-in ROM is also provided to adjust the non-linear characteristics of thermistors.

FAN Tachometer inputs are digital inputs with an acceptable range from 0V to 5V, and are responsible for measuring the FAN's Tachometer pulse periods.

The EC of the IT8720F provides multiple internal registers and an interrupt generator for programmers to monitor the environment and control the FANs. Both the LPC Bus and Serial Bus interfaces are supported to accommodate the needs for various applications.

9.6.1 Interfaces

LPC Bus: The Environment Controller of the IT8720F decodes two addresses.

Table 9-2. Address Map on the LPC Bus

Registers or Port	Address
Address register of the EC	Base+05h
Data register of the EC	Base+06h

Note 1: The Base Address is determined by the Logical Device configuration registers of the Environment Controller (LDN=04h, registers index=60h, 61h).

To access an EC register, the address of the register is written to the address port (Base+05h). Read or write data from or to that register via data port (Base+06h).

9.6.2 Registers

9.6.2.1 Address Port (Base+05h, Default=00h)

Bit	Description
7	Outstanding; read only This bit is set when a data write is performed to Address Port via the LPC Bus.
6-0	Index Internal Address of RAM and Registers

Table 9-3. Environment Controller Registers

Index	R/W	Default	Registers or Action
00h	R/W	18h	Configuration
01h	R	00h	Interrupt Status 1
02h	R	00h	Interrupt Status 2
03h	R	00h	Interrupt Status 3
04h	R/W	00h	SMI# Mask 1
05h	R/W	00h	SMI# Mask 2
06h	R/W	00h	SMI# Mask 3
07h	R/W	00h	Interrupt Mask 1
08h	R/W	00h	Interrupt Mask 2
09h	R/W	80h	Interrupt Mask 3
0Ah	R/W	58h	Interface Selection Register
0Bh	R/W	09h	Fan PWM Smoothing Step Frequency Selection Register
0Ch	R/W	00h	Fan Tachometer 16-bit Counter Enable Register
0Dh	R	-	Fan Tachometer 1 Reading Register
0Eh	R	-	Fan Tachometer 2 Reading Register
0Fh	R	-	Fan Tachometer 3 Reading Register
10h	R/W	-	Fan Tachometer 1 Limit Register
11h	R/W	-	Fan Tachometer 2 Limit Register
12h	R/W	-	Fan Tachometer 3 Limit Register
13h	R/W	07h	Fan Controller Main Control Register
14h	R/W	50h	FAN_CTL Control Register
15h	R/W	00h/20h/40h/7Fh	FAN_CTL1 PWM Control Register
16h	R/W	00h/20h/40h/7Fh	FAN_CTL2 PWM Control Register
17h	R/W	00h/20h/40h/7Fh	FAN_CTL3 PWM Control Register
18h	R	-	Fan Tachometer 1 Extended Reading Register
19h	R	-	Fan Tachometer 2 Extended Reading Register
1Ah	R	-	Fan Tachometer 3 Extended Reading Register
1Bh	R/W	-	Fan Tachometer 1 Extended Limit Register
1Ch	R/W	-	Fan Tachometer 2 Extended Limit Register
1Dh	R/W	-	Fan Tachometer 3 Extended Limit Register
20h	R	-	VIN0 Voltage Reading Register
21h	R	-	VIN1 Voltage Reading Register
22h	R	-	VIN2 Voltage Reading Register
23h	R	-	VIN3 Voltage Reading Register
24h	R	-	VIN4 Voltage Reading Register
25h	R	-	VIN5 Voltage Reading Register
26h	R	-	VIN6 Voltage Reading Register

Index	R/W	Default	Registers or Action
27h	R	-	VIN7 Voltage Reading Register
28h	R	-	VBAT Voltage Reading Register
29h	R	-	TMPIN1 Temperature Reading Register
2Ah	R	-	TMPIN2 Temperature Reading Register
2Bh	R	-	TMPIN3 Temperature Reading Register
30h	R/W	-	VIN0 High Limit Register
31h	R/W	-	VIN0 Low Limit Register
32h	R/W	-	VIN1 High Limit Register
33h	R/W	-	VIN1 Low Limit Register
34h	R/W	-	VIN2 High Limit Register
35h	R/W	-	VIN2 Low Limit Register
36h	R/W	-	VIN3 High Limit Register
37h	R/W	-	VIN3 Low Limit Register
38h	R/W	-	VIN4 High Limit Register
39h	R/W	-	VIN4 Low Limit Register
3Ah	R/W	-	VIN5 High Limit Register
3Bh	R/W	-	VIN5 Low Limit Register
3Ch	R/W	-	VIN6 High Limit Register
3Dh	R/W	-	VIN6 Low Limit Register
3Eh	R/W	-	VIN7 High Limit Register
3Fh	R/W	-	VIN7 Low Limit Register
40h	R/W	-	TMPIN1 High Limit Register
41h	R/W	-	TMPIN1 Low Limit Register
42h	R/W	-	TMPIN2 High Limit Register
43h	R/W	-	TMPIN2 Low Limit Register
44h	R/W	-	TMPIN3 High Limit Register
45h	R/W	-	TMPIN3 Low Limit Register
50h	R/W	00h	ADC Voltage Channel Enable Register
51h	R/W	00h	ADC Temperature Channel Enable Register
52h	R/W	7Fh	TMPIN1 Thermal Output Limit Register
53h	R/W	7Fh	TMPIN2 Thermal Output Limit Register
54h	R/W	7Fh	TMPIN3 Thermal Output Limit Register
55h	R/W	50h	ADC Temperature Extra Channel Enable Register
56h	R/W	00h	Thermal Diode 1 Zero Degree Adjust Register
57h	R/W	00h	Thermal Diode 2 Zero Degree Adjust Register
58h	R	90h	ITE Vendor ID Register
59h	R/W	00h	Thermal Diode 3 Zero Degree Adjust Register
5Bh	R	12h	Core ID Register

Index	R/W	Default	Registers or Action
5Ch	R/W	60h	Beep Event Enable Register
5Dh	R/W	00h	Beep Frequency Divisor of Fan Event Register
5Eh	R/W	00h	Beep Frequency Divisor of Voltage Event Register
5Fh	R/W	00h	Beep Frequency Divisor of Temperature Event Register
60h	R/W	7Fh	FAN_CTL1 SmartGuardian Automatic Mode Temperature Limit of OFF Register
61h	R/W	7Fh	FAN_CTL1 SmartGuardian Automatic Mode Temperature Limit of Fan Start Registers
62h	R/W	7Fh	Reserved Registers
63h	R/W	00h	FAN_CTL1 SmartGuardian Automatic Mode Start PWM Registers
64h	R/W	00h	FAN_CTL1 SmartGuardian Automatic Mode Control Registers
65h	R/W	7Fh	FAN_CTL1 SmartGuardian Automatic Mode Δ -Temperature Registers
68h	R/W	7Fh	FAN_CTL2 SmartGuardian Automatic Mode Temperature Limit of OFF Register
69h	R/W	7Fh	FAN_CTL2 SmartGuardian Automatic Mode Temperature Limit of Fan Start Registers
6Ah	R/W	7Fh	Reserved Registers
6Bh	R/W	00h	FAN_CTL2 SmartGuardian Automatic Mode Start PWM Registers
6Ch	R/W	00h	FAN_CTL2 SmartGuardian Automatic Mode Control Registers
6Dh	R/W	7Fh	FAN_CTL2 SmartGuardian Automatic Mode Δ -Temperature Registers
70h	R/W	7Fh	FAN_CTL3 SmartGuardian Automatic Mode Temperature Limit of OFF Register
71h	R/W	7Fh	FAN_CTL3 SmartGuardian Automatic Mode Temperature Limit of Fan Start Registers
72h	R/W	7Fh	Reserved Registers
73h	R/W	00h	FAN_CTL3 SmartGuardian Automatic Mode Start PWM Registers
74h	R/W	00h	FAN_CTL3 SmartGuardian Automatic Mode Control Registers
75h	R/W	7Fh	FAN_CTL3 SmartGuardian Automatic Mode Δ -Temperature Registers
80h	R	-	Fan Tachometer 4 Reading LSB Register
81h	R	-	Fan Tachometer 4 Reading MSB Register
82h	R	-	Fan Tachometer 5 Reading LSB Register
83h	R	-	Fan Tachometer 5 Reading MSB Register
84h	R/W	-	Fan Tachometer 4 Limit LSB Register
85h	R/W	-	Fan Tachometer 4 Limit MSB Register
86h	R/W	-	Fan Tachometer 5 Limit LSB Register
87h	R/W	-	Fan Tachometer 5 Limit MSB Register
88h	R/W	-0h	External Temperature Sensor Host Status Register
89h	R/W	00h	External Temperature Sensor Host Target Address Register
8Ah	R/W	00h	External Temperature Sensor Host Write Length Register

Index	R/W	Default	Registers or Action
8Bh	R/W	00h	External Temperature Sensor Host Read Length Register
8Ch	R/W	00h	External Temperature Sensor Host Command (Write Data 1) Register
8Dh	R/W	00h	External Temperature Sensor Write Data (2-8) Register
8Eh	R/W	02h	External Temperature Sensor Host Control Register
8Fh	R	00h	External Temperature Sensor Read Data (1-16) Register
90h	R/W	FFh	Special FAN Control Mode Extra Vector A Temperature Limit of Fan Start Register
91h	R/W	00h	Special FAN Control Mode Extra Vector A Slope Register
92h	R/W	00h	Special FAN Control Mode Extra Vector A Δ -Temperature Register
94h	R/W	FFh	Special FAN Control Mode Extra Vector B Temperature Limit of Fan Start Register
95h	R/W	00h	Special FAN Control Mode Extra Vector B Slope Register
96h	R/W	00h	Special FAN Control Mode Extra Vector B Δ -Temperature Register

9.6.2.2 Register Description

9.6.2.2.1 Configuration Register (Index=00h, Default=18h)

Bit	R/W	Description
7	R/W	Initialization A "1" restores all registers to their individual default values, except the Serial Bus Address register. This bit clears itself when the default value is "0".
6	R/W	Update VBAT Voltage Reading
5	R/W	COPEN# Cleared Write "1" to clear COPEN# Note: The COPEN# status register (Index 01h<bit4>) will be cleared when first writing this register and then reading Index 01h<bit4>.
4	R	Read Only; always "1"
3	R/W	INT_Clear A "1" disables the SMI# and IRQ outputs while the contents of interrupt status bits remain unchanged.
2	R/W	IRQ enables the IRQ Interrupt output
1	R/W	SMI# Enable A "1" enables the SMI# Interrupt output.
0	R/W	Start A "1" enables the startup of monitoring operations and a "0" sets the monitoring operation in the STANDBY mode.

9.6.2.2.2 Interrupt Status Register 1 (Index=01h, Default=00h)

Reading this register will clear itself following a read access.

Bit	R/W	Description
7	R	Reserved
6	R	A "1" indicates the FAN_TAC5 Count limit has been reached.
5	R	Reserved
4	R	A "1" indicates a Case Open event has occurred. Note: The COPEN# status register (Index 01h<bit4>) will be cleared when first writing Index 01h<bit4> and then reading this register.
3-0	R	A "1" indicates the FAN_TAC4-1 Count limit has been reached.

9.6.2.2.3 Interrupt Status Register 2 (Index=02h, Default=00h)

Reading this register will clear itself after the read operation is completed.

Bit	R/W	Description
7-0	R	A "1" indicates a High or Low limit of VIN7-0 has been reached.

9.6.2.2.4 Interrupt Status Register 3 (Index=03h, Default=00h)

Reading this register will clear itself following a read access.

Bit	R/W	Description
7-3	R	Reserved
2-0	R	A "1" indicates a High or Low limit of Temperature 3-1 has been reached.

9.6.2.2.5 SMI# Mask Register 1 (Index=04h, Default=00h)

Bit	R/W	Description
7	R/W	Reserved
6	R/W	A "1" disables the FAN_TAC5 interrupt status bit for SMI#.
5	R/W	Reserved
4	R/W	A "1" disables the Case Open Intrusion interrupt status bit for SMI#.
3-0	R/W	A "1" disables the FAN_TAC4-1 interrupt status bit for SMI#.

9.6.2.2.6 SMI# Mask Register 2 (Index=05h, Default=00h)

Bit	R/W	Description
7-0	R/W	A "1" disables the VIN7-0 interrupt status bit for SMI#.

9.6.2.2.7 SMI# Mask Register 3 (Index=06h, Default=00h)

Bit	R/W	Description
7-3	R/W	Reserved
2-0	R/W	A "1" disables the Temperature 3-1 interrupt status bit for SMI#.

9.6.2.2.8 Interrupt Mask Register 1 (Index=07h, Default=00h)

Bit	R/W	Description
7	R/W	Reserved
6	R/W	A "1" disables the FAN_TAC5 interrupt status bit for IRQ.
5	R/W	Reserved
4	R/W	A "1" disables the Case Open Intrusion interrupt status bit for IRQ.
3-0	R/W	A "1" disables the FAN_TAC4-1 interrupt status bit for IRQ.

9.6.2.2.9 Interrupt Mask Register 2 (Index=08h, Default=00h)

Bit	R/W	Description
7-0	R/W	A "1" disables the VIN7-0 interrupt status bit for IRQ.

9.6.2.2.10 Interrupt Mask Register 3 (Index=09h, Default=80h)

Bit	R/W	Description
7	R/W	A "1" disables the External Thermal Sensor interrupt.
6-3	R/W	Reserved
2-0	R/W	A "1" disables the Temperature 3-1 interrupt status bit for IRQ.

9.6.2.2.11 Interface Selection Register (Index=0Ah, Default=58h)

Bit	R/W	Description
7	R/W	Pseudo-EOC (end of conversion of ADC) A Pseudo-EOC bit can speed up the setup time of the FAN speed in the SmartGuardian automatic mode. (Write 1 to the bit then write 0.)
6-4	R/W	External Thermal Sensor Host Selection 000: Disable 100: AMDTSI 101: SST Slave Device 110: PECL 111: SST Host Others: Reserved
3	R/W	SST/PECL Host Controller Clock Selection 0: Internal generated 32M Hz 1: 24MHz
2	R/W	SST/PECL Host Controller (Auto Speed No-change tolerance) t-bit 1 setting 0: (2 host clocks) not shorter than 1 host clock 1: (1 host clock) shorter than 1 host clock
1	R/W	SST/PECL Host Controller Transition Speed Mode Selection 0: Auto 1: Fixed at 0.5Mhz
0	R/W	PECL2.0 Host Controller AWFCFS Enable 0: Disable 1: Enable

9.6.2.2.12 Fan PWM Smoothing Step Frequency Selection Register (Index=0Bh, Default=0Fh)

Bit	R/W	Description
7-6	R/W	FAN PWM Smoothing Step Frequency Selection 00: 16Hz 01: 8Hz 10: 4Hz 11: 2Hz
5-4	R/W	Reserved Must be "00b"
3-2	R/W	FAN_CTL5 Selection 00: Same as FAN_CTL1 01: Same as FAN_CTL2 10: Same as FAN_CTL3 11: None
1-0	R/W	FAN_CTL4 Seletcion 00: The same as FAN_CTL1 01: The same as FAN_CTL2 10: The same as FAN_CTL3 11: None

9.6.2.2.13 Fan Tachometer 16-bit Counter Enable Register (Index=0Ch, Default=00h)

Bit	R/W	Description
7	R/W	TMPIN3 Enhanced Interrupt Mode Enable 0: Original mode 1: The interrupt will be generated when TMPIN3 is higher than the high limit or lower than the low limit.
6	R/W	TMPIN2 Enhanced Interrupt Mode Enable 0: Original mode 1: The interrupt will be generated when TMPIN2 is higher than the high limit or lower than the low limit.
5	R/W	FAN_TAC5 Enable 0: Disable 1: Enable
4	R/W	FAN_TAC4 Enable 0: Disable 1: Enable
3	R/W	TMPIN1 Enhance Interrupt Mode Enable 0: Original mode. 1: The interrupt will be generated when TMPIN1 is higher than the high limit or lower than the low limit.
2	R/W	FAN_TAC3, 16-bit Counter Divisor Enable 0: Disable 1: Enable
1	R/W	FAN_TAC2 16-bit Counter Divisor Enable 0: Disable 1: Enable
0	R/W	FAN_TAC1 16-bit Counter Divisor Enable 0: Disable 1: Enable

9.6.2.2.14 Fan Tachometer 1-3 Reading Registers (Index=0Dh-0Fh)

Bit	R/W	Description
7-0	R	The number of counts of the internal clock per revolution.

9.6.2.2.15 Fan Tachometer 1-3 Limit Registers (Index=10h-12h)

Bit	R/W	Description
7-0	R/W	Limit Value

9.6.2.2.16 Fan Controller Main Control Register (Index=13h, Default=07h)

Bit	R/W	Description
7	R	Reserved
6-4	R/W	FAN_TAC3-1 Enable 0: Disable 1: Enable
3	R/W	Full Speed Control of FAN_CTL Automatic Mode 0: The full speeds of FAN_CTL1-3 automatic mode are independent. 1: All FAN_CTL1-3 will enter the full speed when any temperature exceeds the full Speed Temperature Limit.
2-0	R/W	FAN_CTL3-1 Output Mode Selection 0: ON/OFF mode 1: SmartGuardian mode

9.6.2.2.17 FAN_CTL Control Register (Index=14h, Default=50h)

Bit	R/W	Description
7	R/W	FAN_CTL Polarity (for all FANs) 0: Active low 1: Active high
6-4	R/W	PWM Base Clock Select (for FAN1, 3) 000: 48Mhz (PWM Frequency=375Khz) 001: 24Mhz(PWM Frequency=187.5Khz) 010: 12Mhz(PWM Frequency=93.75Khz) 011: 8Mhz(PWM Frequency=62.5Khz) 100: 6Mhz(PWM Frequency=46.875Khz) 101: 3Mhz(PWM Frequency=23.43Khz) 110: 1.5Mhz(PWM Frequency=11.7Khz) 111: 0.75Mhz(PWM Frequency=5.86Khz)
3	R/W	PWM Minimum Duty Select (for FAN1, 3) 0: 0 % For a given PWM value, the actual duty is PWM/128 X 100%. 1: 20 % For a given PWM value (except 00h), the actual duty is (PWM+32)/160 X 100%. If the given PWM value is 00h, the actual duty will be 0%.
2-0	R/W	FAN_CTL3-1 ON/OFF Mode Control These bits are only available when the relative output modes are selected in the ON/OFF mode. 0: OFF 1: ON

9.6.2.2.18 FAN_CTL1 PWM Control Register (Index=15h, Default=00h/20h/40h/60h)

This default value of this register is selected by JP3 and JP5.

Bit	R/W	Description
7	R/W	FAN_CTL1 PWM Mode Automatic/Software Operation Selection 0: Software operation 1: Automatic operation
6-0	R/W	128 steps of PWM control when in Software operation (bit 7=0), or temperature input selection when in Automatic operation (bit 7=1). Bits[1:0]: 00: TMPIN1 01: TMPIN2 10: TMPIN3 11: Reserved

9.6.2.2.19 FAN_CTL2 PWM Control Register (Index=16h, Default=00h/20h/40h/60h)

This default value of this register is selected by JP3 and JP5.

Bit	R/W	Description
7	R/W	FAN_CTL2 PWM Mode Automatic/Software Operation Selection 0: Software operation 1: Automatic operation
6-0	R/W	128 steps of PWM control when in Software operation (bit 7=0), or temperature input selection when in Automatic operation (bit 7=1). Bits[1:0]: 00: TMPIN1 01: TMPIN2 10: TMPIN3 11: Reserved

9.6.2.2.20 FAN_CTL3 PWM Control Register (Index=17h, Default=00h/20h/40h/60h)

This default value of this register is selected by JP3 and JP5.

Bit	R/W	Description
7	R/W	FAN_CTL3 PWM Mode Automatic/Software Operation Selection 0: Software operation 1: Automatic operation
6-0	R/W	128 steps of PWM control when in Software operation (bit 7=0), or temperature input selection when in Automatic operation (bit 7=1). Bit [1:0]: 00: TMPIN1 01: TMPIN2 10: TMPIN3 11: Reserved

9.6.2.2.21 Fan Tachometer 1-3 Extended Reading Registers (Index=18h-1Ah)

Bit	R/W	Description
7-0	R	Count Number of Internal Clock Per Revolution [15:8]

9.6.2.2.22 Fan Tachometer 1-3 Extended Limit Registers (Index=1Bh-1Dh)

Bit	R/W	Description
7-0	R	Limit Value [15:8]

9.6.2.2.23 VIN7-VIN0 Voltage Reading Registers (Index=27h-20h)

Bit	R/W	Description
7-0	R	Voltage Reading Value

9.6.2.2.24 VBAT Voltage Reading Register (Index=28h)

Bit	R/W	Description
7-0	R	VBAT Voltage Reading Value

9.6.2.2.25 TMPIN3-1 Temperature Reading Registers (Index=2Bh-29h)

Bit	R/W	Description
7-0	R	Temperature Reading Value

9.6.2.2.25.1 VIN7-0 High Limit Registers (Index=3Eh, 3Ch, 3Ah, 38h, 36h, 34h, 32h, 30h)

Bit	R/W	Description
7-0	R/W	High Limit Value

9.6.2.2.26 VIN7-0 Low Limit Registers (Index=3Fh, 3Dh, 3Bh, 39h, 37h, 35h, 33h, 31h)

Bit	R/W	Description
7-0	R/W	Low Limit Value

9.6.2.2.27 TMPIN3-1 High Limit Registers (Index=44h, 42h, 40h)

Bit	R/W	Description
7-0	R/W	High Limit Value

9.6.2.2.28 TMPIN3-1 Low Limit Registers (Index=45h, 43h, 41h)

Bit	R/W	Description
7-0	R/W	Low Limit value

9.6.2.2.29 ADC Voltage Channel Enable Register (Index=50h, Default=00h)

Bit	R/W	Description
7-0	R/W	ADC VIN7-VIN0 Scan Enable

9.6.2.2.30 ADC Temperature Channel Enable Register (Index=51h, Default=00h)

TMPIN3-1 cannot be enabled in both Thermal Resistor mode and Thermal Diode (Diode connected Transistor) mode.

Bit	R/W	Description
7-6	R/W	Reserved
5-3	R/W	TMPIN3-1 is enabled in the Thermal Resistor mode.
2-0	R/W	TMPIN3-1 is enabled in the Thermal Diode (or Diode-connected Transistor) mode.

9.6.2.2.31 TMPIN3-1 Thermal Output Limit Registers (Index=54h-52h, Default=7Fh)

Bit	R/W	Description
7-0	R/W	Thermal Output Limit Value

9.6.2.2.32 ADC Temperature Extra Channel Enable Register (Index=55h, Default=00h)

Bit	R/W	Description
7	R/W	TEMPIN3 Temperature Reading Source Selection 0: TEMPIN3 thermal sensor 1: External Temperature Sensor Host
6-4	R/W	FAN_CTRL2 PWM Base Clock Selection 000: 48Mhz (PWM Frequency=375Khz) 001: 24Mhz(PWM Frequency=187.5Khz) 010: 12Mhz(PWM Frequency=93.75Khz) 011: 8Mhz(PWM Frequency=62.5Khz) 100: 6Mhz(PWM Frequency=46.875Khz) 101: 3Mhz(PWM Frequency=23.43Khz) 110: 1.5Mhz(PWM Frequency=11.7Khz) 111: 0.75Mhz(PWM Frequency=5.86Khz)
3	R/W	FAN_CTRL2 PWM Minimum Duty Selection 0: 0 % For a given PWM value, the actual duty is PWM/128 X 100%. 1: 20 % For a given PWM value (not 00h), the actual duty is (PWM+32)/160 X 100%. If the given PWM value is 00h, the actual duty will be 0%.
2-0	R/W	VIN6-4 is enabled in the Thermal Resistor mode.

9.6.2.2.33 Thermal Diode Zero Degree Adjust 1 Register (Index=56h, Default=00h)

This register is **read only** unless bit 7 of 5Ch is set.

Bit	R/W	Description
7-0	R/W	Thermal Diode 1 Zero Degree Voltage Value

9.6.2.2.34 Thermal Diode Zero Degree Adjust 2 Register (Index=57h, Default=00h)

This register is **read only** unless bit 7 of 5Ch is set.

Bit	R/W	Description
7-0	R/W	Thermal Diode 2 Zero Degree Voltage Value

9.6.2.2.35 Vendor ID Register (Index=58h, Default=90h)

Bit	R/W	Description
7-0	R	ITE Vendor ID; read Only

9.6.2.2.36 Thermal Diode Zero Degree Adjust 3 Register (Index=59h, Default=00h)

This register is **read only** unless bit 7 of 5Ch is set.

Bit	R/W	Description
7-0	R/W	Thermal Diode 3 Zero Degree Voltage Value

9.6.2.2.37 Code ID Register (Index=5Bh, Default=12h)

Bit	R/W	Description
7-0	R	ITE Vendor ID; read Only

9.6.2.2.38 Beep Event Enable Register (Index=5Ch, Default=60h)

Bit	R/W	Description
7	R/W	Thermal Diode Zero Degree Adjust Register Write Enabled
6-4	R/W	ADC clock selector 000: 500Khz 001: 250Khz 010: 125K 011: 62.5Khz 100: 31.25Khz 101: 24Mhz 110: 1Mhz(Default) 111: 2Mhz
3	R/W	Reserved
2	R/W	This bit enables Beep action when TMPINs exceed the limit.
1	R/W	This bit enables Beep action when VINs exceed the limit.
0	R/W	This bit enables Beep action when FAN_TACs exceed the limit.

9.6.2.2.39 Beep Frequency Divisor of Fan Event Register (Index=5Dh, Default=00h)

Bit	R/W	Description
7-4	R/W	Tone Divisor Tone=500/(bits[7:4]+1)
3-0	R/W	Frequency Divisor Frequency=10K/(bits[3:0]+1)

9.6.2.2.40 Beep Frequency Divisor of Voltage Event Register (Index=5Eh, Default=00h)

Bit	R/W	Description
7-4	R/W	Tone Divisor Tone=500/(bits[7:4]+1).
3-0	R/W	Frequency Divisor Frequency=10K/(bits[3:0]+1)

9.6.2.2.41 Beep Frequency Divisor of Temperature Event Register (Index=5Fh, Default=00h)

Bit	R/W	Description
7-4	R/W	Tone Divisor Tone=500/(bits[7:4]+1)
3-0	R/W	Frequency Divisor Frequency=10K/(bits[3:0]+1)

9.6.2.2.42 FAN_CTL3-1 SmartGuardian Automatic Mode Temperature Limit of OFF Registers (Index=70h, 68h, 60h, Default=7Fh)

Bit	R/W	Description
7-0	R/W	Temperature Limit Value of Fan OFF

9.6.2.2.43 FAN_CTL3-1 SmartGuardian Automatic Mode Temperature Limit of Fan Start Registers (Index=71h, 69h, 61h, Default=7Fh)

Bit	R/W	Description
7-0	R/W	Temperature Limit Value of Fan Start

9.6.2.2.44 FAN_CTL3-1 SmartGuardian Automatic Mode Temperature Limit of Full Speed Registers (Index=72h, 6Ah, 62h, Default=7Fh)

Bit	R/W	Description
7-0	R/W	Temperature Limit Value of Fan Full Speed

9.6.2.2.45 FAN_CTL3-1 SmartGuardian Automatic Mode Start PWM Registers (Index=73h, 6Bh, 63h, Default=00h)

Bit	R/W	Description
7	R/W	Slope PWM bit[6] Please refer to the description of SmartGuardian Automatic Mode Control Register.
6-0	R/W	Start PWM Value

9.6.2.2.46 FAN_CTL3-1 SmartGuardian Automatic Mode Control Registers (Index=74h, 6Ch, 64h, Default=00h)

Bit	R/W	Description
7	R/W	FAN Smoothing This bit enables the FAN PWM smoothing changing. 0: Disable 1: Enable
6	R/W	Reserved
5-0	R/W	Slope PWM bit[5:0] Slope = (Slope PWM bit[6:3] + Slope PWM bit[2:0] / 8) PWM value/°C

9.6.2.2.47 FAN_CTL3-1 SmartGuardian Automatic Mode Δ -Temperature Registers (Index=75h, 6Dh, 65h, Default=7Fh)

Bit	R/W	Description
7	R/W	Direct-Down Control This bit selects the PWM linear changing decreasing mode. 0: Slow decreasing mode 1: Direct decreasing mode
6	R/W	FAN full limit control as Thermal out reaching When the relative enable bit is set and the FAN output mode is selected as the automatic mode (bit7 of EC index 15h, 16h, 17h), the relative FAN output will be forced to full PWM if any thermal output limit is reached. 0: Disable 1: Enable
5	-	Reserved
4-0	R/W	Δ -Temperature Interval [4:0]

9.6.2.2.48 Fan Tachometer 4-5 Reading LSB Registers (Index=80h,82h)

Bit	R/W	Description
7-0	R	Count Number of Internal Clock Per Revolution

9.6.2.2.49 Fan Tachometer 4-5 Reading MSB Registers (Index=81h,83h)

Bit	R/W	Description
7-0	R	Count Number of Internal Clock Per Revolution

9.6.2.2.50 Fan Tachometer 4-5 Limit LSB Registers (Index=84h,86h)

Bit	R/W	Description
7-0	R/W	Limit Value

9.6.2.2.51 Fan Tachometer 4-5 Limit MSB Registers (Index=85h,87h)

Bit	R/W	Description
7-0	R/W	Limit Value

9.6.2.2.52 External Temperature Sensor Host Status Register (Index=88h, Default=---00000b)

Bit	R/W	Description
7	R/W	Data FIFO Pointer Clear Writing a 1 to it clears the Read/Write Data FIFO pointers. 0: No action; it always reports 0 when reading it. 1: Both Read and Write Data FIFO pointers will be cleared. Read Data register will point to Read Data 1, and Write Data register will point to Write Data 2.
6	R/WC	SST Bus Abnormal/Contention Error This bit reports the SST/PECL line status. 0: No error 1: Abnormal/Contention error
5	R/WC	SST Slave Message Phase t-bit Extend over Error This bit reports the SST/PECL line status. 0: No error 1: Over specification error
4	R/WC	SST/PECL Line High-Z Status/Failed This bit reports the SST/PECL line High-Z status. 0: SST/PECL line does not drive High-Z. 1: SST/PECL line drives High-Z.
3	R/WC	Write_FCS_ERR Writing a 1 to it clears this bit. In the SST/PECL mode, it reports Write FCS error. It is no use in AMDTSL mode. 0: No Error 1: Write FCS error
2	R/WC	NotValid/Read_FCS_ERR Writing a 1 to it clears this bit. In the AMDTSL mode, it reports valid bit of Data phase. If this bit is 0(valid data =0), the data is valid. In SST/PECL mode, it reports Read FCS error. 0: No Error 1: Read FCS error
1	R/WC	Finish (FNSH) Writing a 1 clears this bit. 0: None 1: This bit is set when the stop condition is detected.
0	R	HOST Busy (BUSY) 0: The current transaction is completed. 1: This bit is set while the command is in operation.

9.6.2.2.53 External Temperature Sensor Host Target Address Register (Index=89h, Default=00h)

Bit	R/W	Description
7-0	R/W	Host Target Address Register (HAddr [7:0]) This register is the Target Address field of the SST/PECL protocol.

9.6.2.2.54 External Temperature Sensor Host Write Length Register (Index=8Ah, Default=00h)

Bit	R/W	Description
7-0	R/W	Host Write Length Register (HW_length [7:0]) This register is the Write Length field of the SST/PECL protocol.

9.6.2.2.55 External Temperature Sensor Host Read Length Register (Index=8Bh, Default=00h)

Bit	R/W	Description
7-0	R/W	Host Read Length Register (HR_length [7:0]) This register is the Read Length field of the SST/PECI protocol.

9.6.2.2.56 External Temperature Sensor Host Command (Write Data 1) Register (Index=8Ch, Default=00h)

Bit	R/W	Description
7-0	R/W	Host Command Register (HCMD [7:0]) This register is the command field of the protocol. In Peci/SST mode, it is the command (Write Data 1) byte. In AMDTSI mode, it is the Command field. If the host controller is busy, the programmer does not change the value of this register, or the host will send the wrong command. If the value is out of definition (for example, 03h to FFh for AMDTSI protocol), the host will transfer it as the normal value and no error will be detected by the host controller.

9.6.2.2.57 External Temperature Sensor Write Data (2-8) Register (Index=8Dh, Default=--h)

Bit	R/W	Description
7-0	R/W	Write Data (2-8) [7:0] (in SST/PECI mode) These registers are only valid in the Peci/SST mode and they are 7-byte FIFO registers.

9.6.2.2.58 External Temperature Sensor Host Control Register (Index=8Eh, Default=02h)

Bit	R/W	Description
7-6	R/W	Auto-Start Control (Auto-START) The host will start the transaction in a regular rate automatically. 00: 32 Hz 01: 16 Hz 10: 8 Hz 11: 4 Hz
5	R/W	Auto-Start (Auto-START) 0: Disable auto-start 1: Enable auto-start The host will start the transaction in a regular rate, which is determined by bit [6:5] automatically.
4	R/W	SST/PECI Host Auto-abort at FCS Error This bit enables the SST/PECI host to abort the transaction when FCS has an error. 0: Disable 1: Enable
3	R/W	Auto-Start Two Domain Enable 0: One Domain 1: Two Domain
2	R/W	SST Contention Control/AMDTSI Clock Selection This bit enables the SST bus contention control. 0: Disable/100kbits/s 1: Enable/400kbits/s When the SST bus is contentious, the host will abort the transaction.

Bit	R/W	Description
1	R/W	SST_idle_High/AMDTSI_byte_sel This bit sets the SST bus idle-high in the SST host mode, or selects 8/16 bit data in the AMDTSI mode. 0: SST Idle Low/AMDTSI 8-bit data 1: SST Idle High/AMDTSI 16-bit data
0	R/W	Start (START) This bit is write-only. Writing 0 to it during transaction will issue a “kill process” and bit4 of 8Bh register will be set. Writing 1 to it during the “NOT BUSY” state (bit0 of 8Bh = 0) will start a transaction. Writing 1 to it during the “BUSY” state (bit0 of 8Bh = 1) will not issue any transaction. So, the programmer should check the “BUSY” status before issuing a transaction. 0: This bit always returns 0 at read. 1: When this bit is set, the host controller will perform the transaction.

9.6.2.2.59 External Temperature Sensor Read Data (1-16) Register (Index=8Fh, Default=--h)

Bit	R/W	Description
7-0	R/W	Read Data (1-16) [7:0] These registers are 16-byte FIFO registers.

9.6.2.2.60 Special FAN Control Mode Extra Vector A, B Temperature Limit of Fan Start Registers (Index=90h, 94h, Default=FFh)

Bit	R/W	Description
7-0	R/W	Temperature Limit Value of Fan Start

9.6.2.2.61 Special FAN Control Mode Extra Vector A, B Slope Registers (Index=91h, 95h, Default=00h)

Bit	R/W	Description
7	R/W	Temperature Input Select 0 Please refer to the description of Special FAN Control Mode Extra Vector A, B Δ -Temperature Registers.
6-0	R/W	Slope PWM bit[6:0] Slope = (Slope PWM bit[6:3] + Slope PWM bit[2:0] / 8) PWM value/ $^{\circ}$ C

9.6.2.2.62 Special FAN Control Mode Extra Vector A, B Δ -Temperature Registers (Index=92h, 96h, Default=00h)

Bit	R/W	Description
7	R/W	Temperature Input Select 1 Temperature input select [1:0]: (Temperature Input Select 0 is bit7 of Special FAN Control mode Extra Vector A, B Slope Registers) 00: TMPIN1 01: TMPIN2 10: TMPIN3 11: Reserve

6-5	R/W	Target FAN Select These bits select the target FAN for the extra-vector to add to. 00: None 01: FAN1 10: FAN2 11: FAN3
4-0	R/W	Δ -Temperature interval [4:0]

9.6.3 Operation

9.6.3.1 Power On RESET and Software RESET

When the system power is first applied, the Environmental Controller performs a “power on reset” on the registers which are returned to default values during a system hardware reset, and the EC will acquire a monitored value before it goes inactive. The ADC is activated to monitor the VBAT pin and then goes inactive. A software reset (bit 7 of Configuration register) performs the same functions as the hardware reset except the function of the Serial Bus Interface Address register.

9.6.3.2 Starting Conversion

The monitoring function in the EC is activated when the bit 3 of Configuration Register is cleared (low) and bit 0 of Configuration Register is set (high). Otherwise, several enabled bits should be set to enable the monitoring function. Those enabled bits are categorized into three groups: positive voltages, temperatures and FAN Tachometer inputs. Before the EC monitoring function can be used, the steps below should be followed:

1. Set the Limits.
2. Set the interrupt Masks.
3. Set the Enable bits.

The EC monitoring process can then be started after these steps.

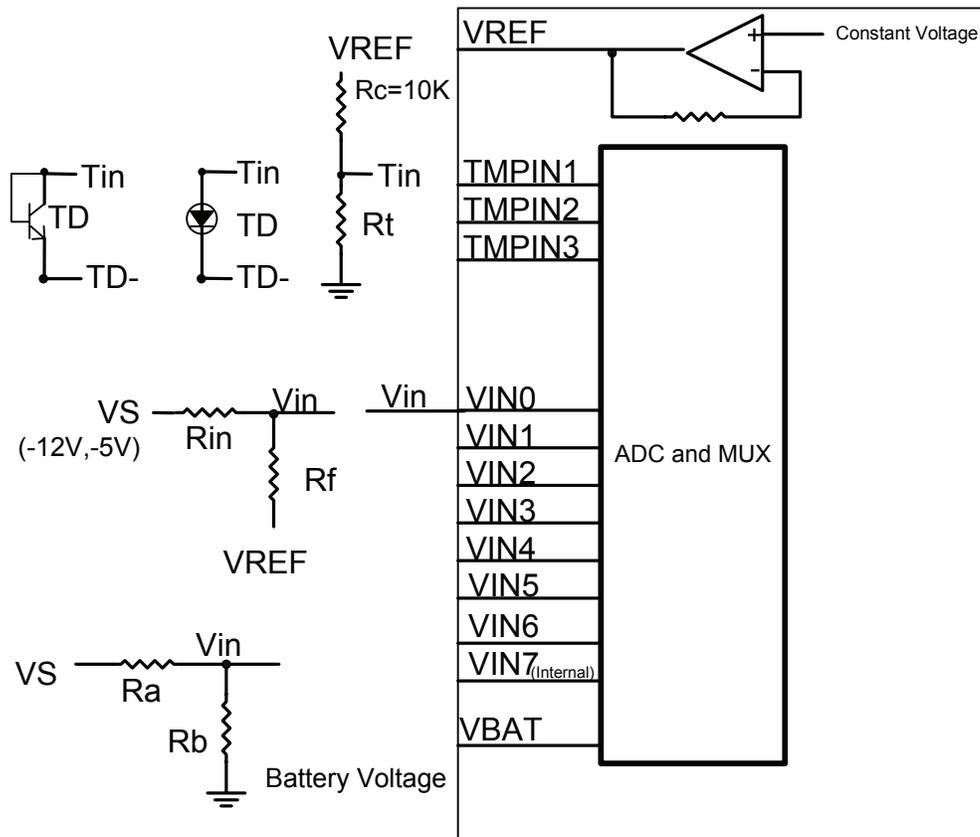


Figure 9-4. Application Example

Note: The resistor should provide approximately 2V at the Analog Inputs.

9.6.3.3 Voltage and Temperature Inputs

The 8-bit ADC has a 16mV LSB with an input range from 0V to 4.096V. The 2.5V and 3.3V supplies of PC applications can be directly connected to the inputs. The 5V and 12V inputs have to be divided into an acceptable range. When the divided circuit is used to measure the positive voltage, the recommended range for Ra and Rb is from 10KΩ to 100KΩ. The negative voltage can be measured by the same divider where the divider is connected to VREF (constant voltage, 4.096V). Do not attempt to measure negative voltage with the divider connected to the ground. The temperature measurement system of the EC converts the voltage of the TMPINs to 8-bit two's-complement. The system also includes an OP amp providing a constant voltage, an external thermistor, a constant resistance, the ADC and a conversion table ROM.

Temperature	Digital Output Format	
	Binary	Hex
+ 125°C	01111101	7Dh
+ 25°C	00011001	19h
+ 1°C	00000001	01h
+ 0°C	00000000	00h
- 1°C	11111111	FFh
- 25°C	11100111	E7h
- 55°C	11001001	C9h

With the addition of the external application circuit, the actual voltages are calculated below:

Positive Voltage: $V_s = V_{in} \times (R_a + R_b) / R_b$

Negative Voltage: $V_s = (1 + R_{in}/R_f) \times V_{in} - (R_{in}/R_f) \times V_{REF}$

All the analog inputs are equipped with the internal diodes that clamp the input voltage exceeding the power supply and ground; nevertheless, the current limiting input resistor is recommended since no dividing circuit is available.

9.6.3.4 Layout and Grounding

A separate and low-impedance ground plane for analog ground is needed to achieve an accurate measurement. The analog ground also provides a ground point for the voltage dividers including the temperature loops and analog components. Analog components such as voltage dividers, feedback resistors and the constant resistors of the temperature loops should be located as closely as possible to the IT8720F. However, the thermistors of the temperature loops should be positioned within the measuring area. In addition, the power supply bypass and the parallel combination of 10 μ F and 0.1 μ F bypass capacitors connected between VCC and analog ground should also be located as closely as possible to the IT8720F.

Due to the small differential voltage of thermal diode (diode-connected transistor), designers should adhere to the following PCB layout's recommendations:

- Position the sensor as closely as possible to the EC.
- The sensor ground should be directly shorted to GNDA with the excellent noise immunity.
- Keep traces away from any noise source. (High voltage, fast data bus, fast clock , CRTs ...)
- Use trace width of 10 mil minimum and provide guard ground (flanking and under).
- Position 0.1 μ F bypass capacitors as closely as possible to the IT8720F.

9.6.3.5 Fan Tachometer

The Fan Tachometer inputs gate a 22.5 kHz clock into an 8-bit or a 16-bit counter (maximum count=255 or 65535) for one period of the input signals. Counts are based on 2 pulses per revolution for tachometer output.

$$\text{RPM} = 1.35 \times 10^6 / (\text{Count} \times \text{Divisor}) ; (\text{Default Divisor} = 2)$$

The maximum input signal range is from 0 to VCC. An additional external circuit is needed to clamp the input voltage and current.

9.6.3.6 Interrupt of the EC

The EC generates interrupts as a result of each of its Limit registers on the analog voltage, temperature, and FAN monitor. All the interrupts are indicated in two Interrupt Status Registers. The IRQ and SMI# outputs have individual mask registers. These two Interrupts can also be enabled/disabled in the Configuration Register. The Interrupt Status Registers will be reset after being read. When the Interrupt Status Registers are cleared, the Interrupt lines will also be cleared. When a read operation is completed before the completion of the monitoring loop sequence, it indicates an Interrupt Status Register has been cleared. The EC needs 1.5 seconds to allow all the EC Registers to be safely updated between completed read operations. When the bit 3 of the Configuration Register is set to high, the Interrupt lines are cleared and the monitoring loop will be stopped. The loop will resume when this bit is cleared.

All the analog voltage inputs have high and low Limit Registers that generate Interrupts. FAN monitoring inputs only have low Limit Register to warn the host. The IT8720F provides three modes dedicated to temperature interrupts in the EC: “Interrupt” mode, “Enhanced Interrupt” mode and “Comparator” mode.

Interrupt Mode

An interrupt will be generated whenever the temperature exceeds Th limit, and the corresponding interrupt status bits will be set to high until being reset by reading Interrupt Status Register 3. Once an interrupt event occurs by exceeding Th limit, an interrupt will only occur again when the temperature goes below TL limit after being reset. Again, it will set the corresponding status bit to high until being reset by reading the Interrupt Status Register 3.

Enhanced Interrupt Mode

When the enhanced interrupt mode is enabled (bits 3, 6 and 7 of EC index 0Ch for TMPIN1, 2, and 3 respectively), an interrupt will be generated when the temperature is higher than the high limit or lower than the low limit.

Comparator Mode

This mode is entered when the TL limit register is set to 127°C. In this mode, an interrupt will be generated whenever the temperature exceeds the Th limit. The interrupt will also be cleared by reading the Interrupt Status Register 3, but the interrupt will be set again following the completion of another measurement cycle. It will remain set until the temperature goes below the Th limit.

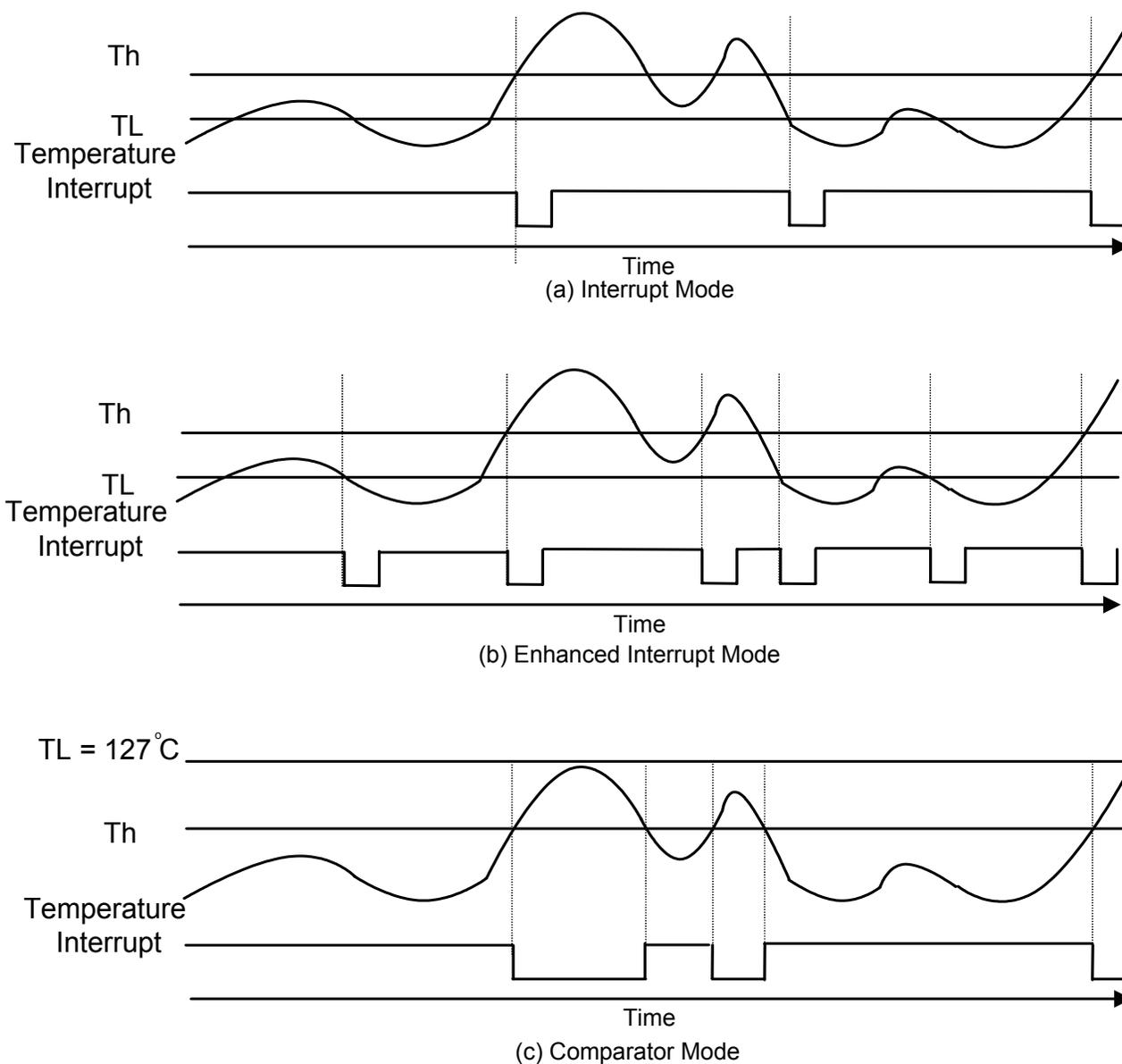


Figure 9-5. Temperature Interrupt Response Diagram

9.6.3.7 FAN Controller FAN_CTL's ON-OFF and SmartGuardian Modes

The IT8720F provides an advanced FAN Controller. Two modes, ON_OFF and SmartGuardian, are provided for each controller. The former is a logical ON or OFF, and the latter is a PWM output. With the addition of external application circuits, the FAN's voltage values can be varied easily.

In the SmartGuardian Mode, there are two operational choices, software control or automatic control.

While under software control, the PWM value is subject to the changes in the values of bits 6-0 of FAN_CTL 1-3 PWM Control Registers (Index=15h, 16h, 17h). With the application circuits, FAN_CTL can generate 128 steps of the voltage. So, the FAN_CTL 1-3 PWM Control Registers can vary the voltage by changing the PWM value. Fan speeds or other voltage control cooling device can be varied in 128 steps.

While under automatic mode, the PWM value is subject to the temperature inputs by linear changes. When the temperature exceeds a start limit, FAN_CTL spins in a start PWM value (Index 73h, 6Bh, 63h). When the temperature reading is between the Start limit and the full limit ($=T_s+(128- \text{Start PWM})/\text{Slope}$), the PWM value changes depending on the temperature reading if the reading exceeds the right boundary. If the temperature increases $X\text{ }^\circ\text{C}$, the PWM value will increase $X * K$. K (Slope) is a constant value with 4 bits for the integer and 3 bits for the decimal, and is determined in bit 7 of FAN_CTL 3-1 SmartGuardian Automatic mode Start PWM register and bits 5-0 of FAN_CTL 3-1 SmartGuardian Automatic mode control registers. However, if the reading doesn't exceed the right boundary, the PWM value will keep the original value. For example, if PWM is currently at a value of P_a , it will not change if $T_b < \text{the temperature reading} < T_a$. If the new reading (T_{new}) $> T_a$, the new PWM value will be $\text{Start PWM} + K * (T_{\text{new}} - T_s)$. If the new reading $< T_b$, there are two decreasing modes. If bit 7 of FAN_CTL 3-1 SmartGuardian Automatic mode Δ -Temperature is 0, the new PWM value will be $\text{Start PWM} + K * ((T_{\text{new}}+T_a)/2 - T_s)$. If the bit is 1, the new PWM value will be $\text{Start PWM} + K * (T_{\text{new}} - T_s)$. When the temperature is lower than the start limit but larger than the OFF limit (Index 70h, 68h, 60h), FAN_CTL will not stop, but keep in the start PWM value until the temperature is lower than the OFF limit.

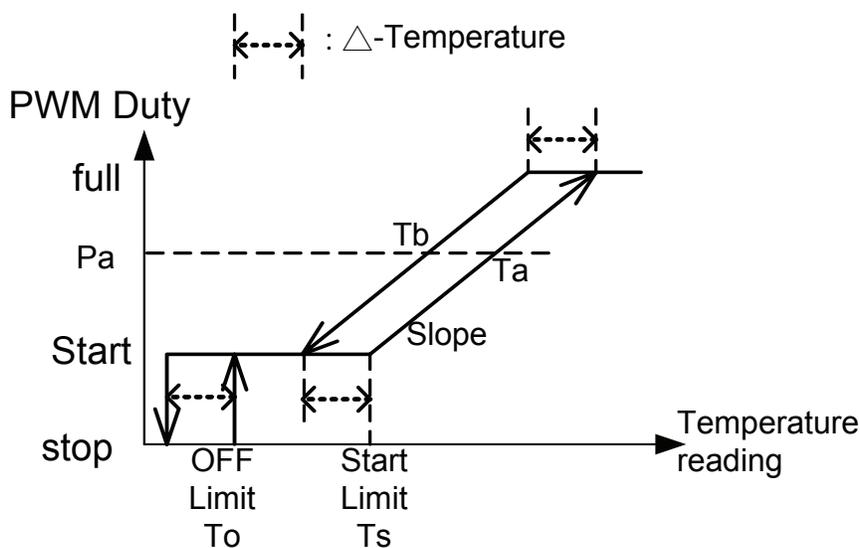


Figure 9-6. SmartGuardian Automatic Mode

9.7 Floppy Disk Controller (FDC)

9.7.1 Introduction

The Floppy Disk Controller provides the interface between a host processor and up to two floppy disk drives. It integrates a controller and a digital data separator with write precompensation, data rate selection logic, microprocessor interface, and a set of registers.

The FDC supports data transfer rates of 250 Kbps, 300 Kbps, 500 Kbps, and 1 Mbps. It operates in the PC/AT mode and supports 3-mode type drives. Additionally, the FDC is software compatible with the 82077.

The FDC configuration is handled by software and a set of Configuration registers. Status, Data, and Control registers facilitate the interface between the host microprocessor and the disk drive, providing information about the condition and/or state of the FDC. These configuration registers can select the data rate, enable interrupts, drives, and DMA modes, and indicate errors in the data or operation of the FDC/FDD.

The controller manages data transfer using a set of data transfer and control commands. These commands are handled in three phases: Command, Execution, and Result. Not all commands utilize all these three phases.

9.7.2 Reset

The IT8720F device implements both software and hardware reset options for the FDC. Either option will reset the FDC, terminating all operations and placing the FDC into an idle state. A reset during a write to the disk will corrupt the data and the corresponding CRC.

9.7.3 Hardware Reset (LRESET# Pin)

When the FDC receives an LRESET# signal, all registers of the FDC core are cleared, except those programmed by the SPECIFY command. To exit the reset state, the host must clear the DOR bit.

9.7.4 Software Reset (DOR Reset and DSR Reset)

When the reset bit in the DOR or the DSR is set, all registers of the FDC core are cleared. A reset performed by setting the reset bit in the DOR has a higher priority over a reset performed by setting the reset bit in the DSR. In addition, to exit the reset state, the DSR bit is self-clearing while the host must clear the DOR bit.

9.7.5 Digital Data Separator

The internal digital data separator is comprised of a digital PLL and associated support circuitry. It is responsible for synchronizing the raw data signal read from the floppy disk drive. The synchronized signal is used to separate the encoded clock from the data pulses.

9.7.6 Write Precompensation

Write precompensation is a method that can be used to adjust the effects of bit shifting on data as it is written to the disk. It is harder for the data separator to read data that have been subject to bit shifting. Soft read errors can occur due to such bit shifting. Write precompensation predicts where the bit shifting might occur within a data pattern and shifts the individual data bits back to their nominal positions.

The FDC permits the selection of write precompensation via the Data Rate Select Register (DSR) bits 2 through 4.

9.7.7 Data Rate Selection

Selecting one of the four possible data rates for the attached floppy disks is accomplished by setting the Diskette Control Register (DCR) or Data Rate Select Register (DSR) bits to 0 and 1. The data rate is determined by the last value that is written to either the DCR or the DSR. When the data rate is set, the data separator clock is scaled appropriately.

9.7.8 Status, Data and Control Registers

9.7.8.1 Digital Output Register (DOR, FDC Base Address + 02h)

This is a **read/write** register. It controls drive selection and motor enable as well as a software reset bit and DMA enable. The I/O interface reset may be used at any time to clear the DOR's contents.

Table 9-4. Digital Output Register (DOR)

Bit	Symbol	Description
7-6	-	Reserved
5	MOTB EN	Drive B Motor Enable 0: Disable Drive B motor 1: Enable Drive B motor
4	MOTA EN	Drive A Motor Enable 0: Disable Drive A motor 1: Enable Drive A motor
3	DMAEN	Disk Interrupt and DMA Enable 0: Disable disk interrupt and DMA (DRQx, DACKx#, TC and INTx) 1: Enable disk interrupt and DMA
2	RESET#	FDC Function Reset 0: Reset FDC function 1: Clear reset of FDC function This reset does not affect the DSR, DCR or DOR.
1	-	Reserved
0	DVSEL	Drive Selection 0: Select Drive A 1: Select Drive B

9.7.8.2 Tape Drive Register (TDR, FDC Base Address + 03h)

This is a **read/write** register and is included for 82077 software compatibility. The contents of this register are not used internally to the device.

Table 9-5. Tape Drive Register (TDR)

Bit	Symbol	Description
7-2	-	Reserved
1-0	TP_SEL[1:0]	Tape Drive Selection TP_SEL[1:0] : Drive selected 00: None 01: 1 10: 2 11: 3

9.7.8.3 Main Status Register (MSR, FDC Base Address + 04h)

This is a **read only** register. It indicates the general status of the FDC, and is able to receive data from the host. The MSR should be read before each byte is sent to or received from the Data register, except when it is in the DMA mode.

Table 9-6. Main Status Register (MSR)

Bit	Symbol	Description
7	RQM	Request for Master FDC Request for Master 0: The FDC is busy and cannot receive data from the host. 1: The FDC is ready and the host can transfer data.
6	DIO	Data I/O Direction Indicates the direction of data transfer once an RQM has been set. 0: Write 1: Read
5	NDM	Non-DMA Mode This bit selects Non-DMA mode of operation. 0: DMA mode selected 1: Non-DMA mode selected This mode is selected via the SPECIFY command during the Execution phase of a command.
4	CB	Diskette Control Busy Indicates whether a command is in progress (the FDD is busy). 0: A command has been executed and the end of the Result phase has been reached. 1: A command is being executed.
3-2	-	Reserved
1	DBB	Drive B Busy Indicates whether Drive B is in the SEEK portion of a command. 0: Not busy 1: Busy
0	DAB	Drive A Busy Indicates whether Drive A is in the SEEK portion of a command. 0: Not busy 1: Busy

9.7.8.4 Data Rate Select Register (DSR, FDC Base Address + 04h)

This is a **write only** register. It is used to determine the data rate, amount of write precompensation, power down mode, and software reset. The data rate of the floppy disk controller is the most recent write of either the DSR or DCR. The DSR is unaffected by a software reset. The DSR can be set to 02h by a hardware reset. The "02h" represents the default precompensation, and 250 Kbps indicates the data transfer rate.

Table 9-7. Data Rate Select Register (DSR)

Bit	Symbol	Description
7	S/W RESET	Software Reset It is active high and shares the same function with the RESET# of the DOR, except that this bit is self-clearing.
6	POWER DOWN	Power Down When 1 is written to this bit, the floppy controller is put into the manually low-power mode. The clocks of the floppy controller and data separator circuits will be turned off until software reset, Data Register or Main Status Register is accessed.

Bit	Symbol	Description																												
5	-	Reserved																												
4-2	PRE-COMP 2-0	<p>Precompensation Select These three bits are used to determine the value of write precompensation that will be applied to the WDATA# pin. Track 0 is the default starting track number, which can be changed by the CONFIGURE command for precompensation.</p> <table border="1"> <thead> <tr> <th>PRE_COMP</th> <th>Precompensation Delay</th> </tr> </thead> <tbody> <tr><td>111</td><td>0.0 ns</td></tr> <tr><td>001</td><td>41.7 ns</td></tr> <tr><td>010</td><td>83.3 ns</td></tr> <tr><td>011</td><td>125.0 ns</td></tr> <tr><td>100</td><td>166.7 ns</td></tr> <tr><td>101</td><td>208.3 ns</td></tr> <tr><td>110</td><td>250.0 ns</td></tr> <tr><td>000</td><td>Default</td></tr> </tbody> </table> <p>Default Precompensation Delays</p> <table border="1"> <thead> <tr> <th>Data Rate</th> <th>Precompensation Delay</th> </tr> </thead> <tbody> <tr><td>1 Mbps</td><td>41.7 ns</td></tr> <tr><td>500 Kbps</td><td>125.0 ns</td></tr> <tr><td>300 Kbps</td><td>125.0 ns</td></tr> <tr><td>250 Kbps</td><td>125.0 ns</td></tr> </tbody> </table>	PRE_COMP	Precompensation Delay	111	0.0 ns	001	41.7 ns	010	83.3 ns	011	125.0 ns	100	166.7 ns	101	208.3 ns	110	250.0 ns	000	Default	Data Rate	Precompensation Delay	1 Mbps	41.7 ns	500 Kbps	125.0 ns	300 Kbps	125.0 ns	250 Kbps	125.0 ns
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00	500 Kbps																													
01	300 Kbps																													
10	250 Kbps (default)																													
11	1 Mbps																													

9.7.8.5 Data Register (FIFO, FDC Base Address + 05h)

This is an 8-bit **read/write** register. It transfers command information, diskette drive status information, and the result phase status between the host and the FDC. The FIFO consists of several registers in a stack. Only one register in the stack is permitted to transfer the information or status to the data bus at a time.

Table 9-8. Data Register (FIFO)

Bit	Symbol	Description
7-0	-	Data Command information, diskette drive status, or result phase status data.

9.7.8.6 Digital Input Register (DIR, FDC Base Address + 07h)

This is a **read only** register and shares this address with the Diskette Control Register (DCR).

Table 9-9. Digital Input Register (DIR)

Bit	Symbol	Description
7	DSKCHG	Diskette Change Indicates the inverting value of the bit monitored from the input of the Floppy Disk Change pin (DSKCHG#).
6-0	-	Reserved

9.7.8.7 Diskette Control Register (DCR, FDC Base Address + 07h)

This is a **write only** register and shares this address with the Digital Input Register (DIR). The DCR register controls the data transfer rate for the FDC.

Table 9-10. Diskette Control Register (DCR)

Bit	Symbol	Description										
7-2	-	Reserved Always 0										
1-0	DRATE1-0	Data Rate Select <table style="margin-left: 40px;"> <thead> <tr> <th>Bits 1-0</th> <th>Data Transfer Rate</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>500 Kbps</td> </tr> <tr> <td>01</td> <td>300 Kbps</td> </tr> <tr> <td>10</td> <td>250 Kbps</td> </tr> <tr> <td>11</td> <td>1 Mbps</td> </tr> </tbody> </table>	Bits 1-0	Data Transfer Rate	00	500 Kbps	01	300 Kbps	10	250 Kbps	11	1 Mbps
Bits 1-0	Data Transfer Rate											
00	500 Kbps											
01	300 Kbps											
10	250 Kbps											
11	1 Mbps											

9.7.9 Controller Phases

The FDC handles data transfer and control commands in three phases, Command, Execution and Result. Not all commands utilize these three phases.

9.7.9.1 Command Phase

Upon reset, the FDC enters the Command phase and is ready to receive commands from the host. The host must verify that MSR bit 7 (RQM) = 1 and MSR bit 6 (DIO) = 0, indicating the FDC is ready to receive data. For each command, a defined set of command code and parameter bytes must be transferred to the FDC in a given order. See sections 9.7.11 Data Transfer Commands and 9.7.12 Control Commands for details of various commands. RQM is set false (0) after each byte-Read cycle, and set true (1) when a new parameter byte is required. The Command phase is completed when this set of bytes has been received by the FDC. The FDC automatically enters the next controller phase and the FIFO is disabled.

9.7.9.2 Execution Phase

Upon the completion of the Command phase, the FDC enters the Execution phase. It is in this phase that all data transfer occurs between the host and the FDC. The SPECIFY command indicates whether this data transfer occurs in the DMA or non-DMA mode. Each data byte is transferred via an IRQx or DRQx# based upon the DMA mode. On reset, the CONFIGURE command can automatically enable or disable the FIFO. The Execution phase is completed when all data bytes have been received. If the command executed does not require a Result phase, the FDC is ready to receive the next command.

9.7.9.3 Result Phase

For commands that require data written to the FIFO, the FDC enters the Result phase when the IRQ or DRQ is activated. The MSR bit 7 (RQM) and MSR bit 6 (DIO) must equal to 1 to read the data bytes. The Result phase is completed when the host has read each of the defined set of result bytes for the given command. Right after the completion of the phase, RQM is set to 1, DIO is set to 0, and the MSR bit 4 (CB) is cleared, indicating the FDC is ready to receive the next command.

9.7.9.4 Result Phase Status Registers

For commands that contain a Result phase, these **read only** registers indicate the status of the most recently executed command.

Table 9-11. Status Register 0 (ST0)

Bit	Symbol	Description
7-6	IC	Interrupt Code 00: The execution of the command has been completed correctly. 01: The execution of the command is activated but fails to be completed successfully. 10: It means an invalid command. 11: The execution of the command is not completed correctly due to a polling error.
5	SE	Seek End The FDC executes a SEEK or RE-CALIBRATE command.
4	EC	Equipment Check The TRK0# pin is not set after a RE-CALIBRATE command is issued.
3	NU	Not Used
2	H	Head Address The current head address
1	DSB	Drive B Select
0	DSA	Drive A Select

Table 9-12. Status Register 1 (ST1)

Bit	Symbol	Description
7	EN	End of Cylinder Indicates the FDC attempts to access a sector beyond the final sector of the track. This bit will be set if the Terminal Count (TC) signal is not issued after a READ DATA or WRITE DATA command.
6	NU	Not Used
5	DE	Data Error A CRC error occurs in either the ID field or the data field of a sector.
4	OR	Overrun/Underrun An overrun on a READ operation or underrun on a WRITE operation occurs when the FDC is not serviced by the CPU or DMA within the required time interval.
3	NU	Not Used
2	ND	No Data No data are available to the FDC when either of the following conditions is met: The floppy disk cannot find the indicated sector while the READ DATA or READ DELETED DATA commands are being executed. While a READ ID command is being executed, an error occurs upon reading the ID field.

Bit	Symbol	Description
		While a READ A TRACK command is being executed, the FDC cannot find the starting sector.
1	NW	Not Writeable It is set when WRITE DATA, WRITE DELETED DATA, or FORMAT A TRACK command is being executed on a write-protected diskette.
0	MA	Missing Address Mark This flag bit is set when either of the following conditions is met: The FDC cannot find a Data Address Mark or a Deleted Data Address Mark on the specified track. The FDC cannot find any ID address on the specified track after two index pulses are detected from the INDEX# pin.

Table 9-13. Status Register 2 (ST2)

Bit	Symbol	Description
7	NU	Not Used
6	CM	Control Mark This flag bit is set when either of the following conditions is met: 1. The FDC finds a Deleted Data Address Mark during a READ DATA command. 2. The FDC finds a Data Address Mark during a READ DELETED DATA command.
5	DD	Data Error in Data Field This flag bit is set when a CRC error is found in the data field.
4	WC	Wrong Cylinder This flag bit is set when the track address in the ID field is different from the track address specified in the FDC.
3	SH	Scan Equal Hit This flag bit is set when the condition of "equal" is satisfied during a SCAN command.
2	SN	Scan Not Satisfied This flag bit is set when the FDC cannot find a sector on the cylinder during a SCAN command.
1	BC	Bad Cylinder This flag bit is set when the track address equals to "FFh" and is different from the track address in the FDC.
0	MD	Missing Data Address Mark This flag bit is set when the FDC cannot find a Data Address Mark or Deleted Data Address Mark.

Table 9-14. Status Register 3 (ST3)

Bit	Symbol	Description
7	FT	Fault Indicates the current status of the Fault signal from the FDD.
6	WP	Write Protect Indicates the current status of the Write Protect signal from the FDD.
5	RDY	Ready Indicates the current status of the Ready signal from the FDD.
4	TK0	Track 0 Indicates the current status of the Track 0 signal from the FDD.
3	TS	Two Side Indicates the current status of the Two Side signal from the FDD.
2	HD	Head Address

Bit	Symbol	Description
		Indicates the current status of the Head Select signal to the FDD.
1-0	US1, US0	Unit Select Indicates the current status of the Unit Select signals to the FDD.

9.7.10 Command Set

The FDC utilizes a defined set of commands to communicate with the host. Each command is comprised of a unique first byte containing the op-code, and a series of additional bytes containing the required set of parameters and results. The descriptions use a common set of parameter byte symbols, which are presented in the following table. The FDC commands may be executed whenever the FDC is in the Command phase. The FDC will check whether the first byte is a valid command or not. If yes, it will proceed. If not, an interrupt will be issued.

Table 9-15. Command Set Symbol Descriptions

Symbol	Description
C	Cylinder Number The current/selected cylinder (track) number: 0-255.
D	Data The data pattern to be written into a sector.
DC3-DC0	Drive Configuration Bit 3-0 Designate which drives are the perpendicular drives on the PERPENDICULAR MODE command.
DIR	Direction Control Read/Write Head Step Direction Control. 0 = Step Out; 1 = Step In.
DR0, DR1	Disk Drive Select The selected drive number: 0 or 1.
DTL	Data Length When N is defined as 00h, DTL designates the number of data bytes which users are going to read out or write into the Sector. When N is not 00h, DTL is undefined.
DFIFO	Disable FIFO A "1" will disable the FIFO (default) and a "0" will enable it.
EC	Enable Count If EC=1, DTL of VERIFY command will be SC.
EIS	Enable Implied Seek If EIS=1, a SEEK operation will be performed before executing any READ or WRITE command that requires the C parameter.
EOT	End of Track The final sector number on a cylinder. During a READ or WRITE operation, the FDC stops data transfer after the sector number is equal to EOT.
GAP2	Gap 2 Length By PERPENDICULAR MODE command, this parameter changes the format of the length of Gap 2.
GPL	Gap Length The length of Gap 3. During a FORMAT command, it determines the size of Gap 3.
H	Head Address The Head number 0 or 1, as specified in the sector ID field. (H = HD in all command words.)
HD	Head The selected Head number: 0 or 1. It also controls the polarity of HDSEL#. (H = HD in all command words.)
HLT	Head Load Time The Head Load Time in the FDD (2 to 254 ms in 2 ms increments).
HUT	Head Unload Time

	The Head Unload Time after a READ or WRITE operation has been executed (16 to 240 ms in 16 ms increments).
--	--

Symbol	Description
LOCK	If LOCK=1, DFIFO, FIFOTHR, and PRETRK parameters of the CONFIGURE command will not be affected by a software reset. If LOCK=0 (default), the above parameters will be set to their default values following a software reset.
MFM	FM or MFM Mode If MFM is low, FM Mode (single density) is selected. If MFM is high, MFM Mode (double density) is selected.
MT	Multi-Track If MT is high, a Multi-Track operation will be performed. In this mode, the FDC will automatically start searching for sector 1 on side 1 after finishing a READ/WRITE operation in the last sector on side 0.
N	Number The number of data bytes written into a sector, where: 00: 128 bytes (PC standard) 01: 256 bytes 02: 512 bytes ... 07: 16 Kbytes
NCN	New Cylinder Number A new cylinder number, which is to be reached as a result of the SEEK operation. Desired position of Head.
ND	Non-DMA Mode When ND is high, the FDC operates in the Non-DMA Mode.
OW	Overwrite If OW=1, DC3-0 of the PERPENDICULAR MODE command can be modified. Otherwise, those bits cannot be changed.
PCN	Present Cylinder Number The cylinder number at the completion of a SENSE INTERRUPT STATUS command. Position of Head at present time.
POLL	Polling Disable If POLL=1, the internal polling routine is disabled.
PRETRK	Precompensation Starting Track Number Programmable from track 0-255.
R	Record The sector number to be read or written
RCN	Relative Cylinder Number To determine the relative cylinder offset from present cylinder used by the RELATIVE SEEK command.
SC	Number of Sector Per Cylinder
SK	Skip If SK=1, the Read Data operation will skip sectors with a Deleted Data Address Mark. Otherwise, the Read Deleted Data operation only accesses sectors with a Deleted Data Address Mark.
SRT	Step Rate Time The stepping rate for the FDD (1 to 16 ms in 1 ms increments). The stepping rate is applied to all drives (F=1 ms, E=2 ms, etc.).

Table 9-15. Command Set Symbol Descriptions [cont'd]

Symbol	Description
ST0 ST1 ST2 ST3	Status 0 Status 1 Status 2 Status 3 ST0-3 stand for one of four registers that store the status information after a command has been executed. This information is available during the Result phase after command execution. These registers should not be confused with the Main Status Register (selected by A ₀ = 0). ST0-3 may be read only after a command has been executed and contain information associated with that particular command.
STP	If STP = 1 during a SCAN operation, the data in contiguous sectors are compared byte by byte with data sent from the processor (or DMA). If STP = 2, alternate sectors are read and compared.

Table 9-16. Command Set Summary

READ DATA											
Phase	R/W	Data Bus								Remarks	
		D7	D6	D5	D4	D3	D2	D1	D0		
Command	W	MT	MFM	SK	0	0	1	1	0	Command Codes	
	W	0	0	0	0	0	HDS	DR1	DR0		
	W	C									Sector ID information before the command execution
	W	H									
	W	R									
	W	N									
	W	EOT									
	W	GPL									
W	DTL										
Execution										Data transfer between the FDD and the main system	
Result	R	ST0								Status information after command execution	
	R	ST1									
	R	ST2									
	R	C								Sector ID information after command execution	
	R	H									
	R	R									
	R	N									

READ DELETED DATA										
Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	MT	MFM	SK	0	1	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
	W	C								Sector ID information before the command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								

READ A TRACK										
Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	MFM	0	0	0	0	1	0	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
	W	C								Sector ID information before the command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								

WRITE DATA										
Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	MT	MFM	0	0	0	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
	W	C								Sector ID information before the command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								
	R									

WRITE DELETED DATA										
Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	MT	MFM	0	0	1	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
	W	C								Sector ID information before the command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								
	R									

FORMAT A TRACK										
Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	MFM	0	0	1	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
	W	N								Bytes/Sector
	W	SC								Sectors/Cylinder
	W	GPL								Gap 3
	W	D								Filler Byte
Execution	W	C								Input Sector Parameters per-sector FDC formats an entire cylinder
	W	H								
	W	R								
	W	N								
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	Undefined								
	R	Undefined								
	R	Undefined								
	R	Undefined								

SCAN EQUAL										
Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	MT	MFM	SK	1	0	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
	W	C								Sector ID information before the command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transferred from the system to controller is compared to data read from disk
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								

SCAN LOW OR EQUAL											
Phase	R/W	Data Bus								Remarks	
		D7	D6	D5	D4	D3	D2	D1	D0		
Command	W	MT	MFM	SK	1	1	0	0	1	Command Codes	
	W	0	0	0	0	0	HDS	DR1	DR0		
	W	C									Sector ID information before the command execution
	W	H									
	W	R									
	W	N									
	W	EOT									
	W	GPL									
	W	DTL									
Execution										Data transferred from the system to controller is compared to data read from disk	
Result	R	ST0								Status information after command execution	
	R	ST1									
	R	ST2									
	R	C								Sector ID information after command execution	
	R	H									
	R	R									
	R	N									

SCAN HIGH OR EQUAL											
Phase	R/W	Data Bus								Remarks	
		D7	D6	D5	D4	D3	D2	D1	D0		
Command	W	MT	MFM	SK	1	1	1	0	1	Command Codes	
	W	0	0	0	0	0	HDS	DR1	DR0		
	W	C									Sector ID information before the command execution
	W	H									
	W	R									
	W	N									
	W	EOT									
	W	GPL									
	W	DTL									
Execution										Data transferred from the system to controller is compared to data read from disk	
Result	R	ST0								Status information after command execution	
	R	ST1									
	R	ST2									
	R	C								Sector ID information after command execution	
	R	H									
	R	R									
	R	N									

VERIFY											
Phase	R/W	Data Bus								Remarks	
		D7	D6	D5	D4	D3	D2	D1	D0		
Command	W	MT	MFM	SK	1	0	1	1	0	Command Codes	
	W	EC	0	0	0	0	HDS	DR1	DR0		
	W	C									Sector ID information before the command execution
	W	H									
	W	R									
	W	N									
	W	EOT									
	W	GPL									
W	DTL/SC										
Execution										No data transfer takes place	
Result	R	ST0								Status information after command execution	
	R	ST1									
	R	ST2									
	R	C								Sector ID information after command execution	
	R	H									
	R	R									
	R	N									

READ ID										
Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	MFM	0	0	1	0	1	0	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
Execution										The first correct ID information on the Cylinder is stored in the Data Register
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information during execution phase
	R	H								
	R	R								
	R	N								

CONFIGURE											
Phase	R/W	Data Bus								Remarks	
		D7	D6	D5	D4	D3	D2	D1	D0		
Command	W	0	0	0	1	0	0	1	1	Configure Information	
	W	0	0	0	0	0	0	0	0		
	W	0	EIS	DFIFO	POLL	FIFOTHR					
		PRETRK									
Execution											

RE-CALIBRATE										
Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	0	0	1	1	1	Command Codes
	W	0	0	0	0	0	0	DR1	DR0	
Execution										Head retracted to Track 0

SEEK										
Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	0	1	1	1	1	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
	W	NCN								
Execution										Head is positioned over proper cylinder on diskette

RELATIVE SEEK										
Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	1	DIR	0	0	1	1	1	1	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
	W	RCN								
Execution										Head is stepped in or out a programmable number of tracks

DUMPREG											
Phase	R/W	Data Bus								Remarks	
		D7	D6	D5	D4	D3	D2	D1	D0		
Command	W	0	0	0	0	1	1	1	0	Command Codes	
Execution										Registers placed in FIFO	
Result	R	PCN-Drive 0									
	R	PCN-Drive 1									
	R	PCN-Drive 2									
	R	PCN-Drive 3									
	R	SRT				HUT					
	R	HLT									ND
	R	SC/EOT									
	R	LOCK	0	DC3	DC2	DC1	DC0	GAP	WG		
	R	0	DIS	DFIFO	POLLD	FIFOTHR					
	R	PRETRK									

LOCK										
Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	LOCK	0	0	1	0	1	0	0	Command Codes
Result	R	0	0	0	LOCK	0	0	0	0	

VERSION										
Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	1	0	0	0	0	Command Codes
Result	R	1	0	0	1	0	0	0	0	Enhanced Controller

SENSE INTERRUPT STATUS										
Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	0	1	0	0	0	Command Codes
Result	R	ST0								Status information at the end of each SEEK operation
	R	PCN								

SENSE DRIVE STATUS										
Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	0	0	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
Result	R	ST3								Status information about FDD

SPECIFY										
Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	0	0	0	1	1	Command Codes
	W	SRT				HUT				
	W	HLT							ND	

PERPENDICULAR MODE										
Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	1	0	0	1	0	Command Codes
	W	OW	0	DC3	DC2	DC1	DC0	GAP	WG	

INVALID										
Phase	R/W	Data Bus								Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	Invalid codes								INVALID Command Codes (NO-OP: FDC goes into the standby state)
Result	R	ST0								ST0 = 80h

9.7.11 Data Transfer Commands

All data transfer commands utilize the same parameter bytes (except for FORMAT A TRACK command) and return the same result data bytes. The only difference between them is the five bits (bit 0-bit 4) of the first byte.

9.7.11.1 Read Data

The READ DATA command contains nine command bytes that place the FDC into the Read Data mode. Each READ operation is initialized by a READ DATA command. The FDC locates the sector to be read by matching ID Address Marks and ID fields from the command with the information on the diskette. The FDC then transfers the data to the FIFO. When the data from the given sector have been read, the READ DATA command is completed and the sector address is automatically incremented by 1. The data from the next sector are read and transferred to the FIFO in the same manner. Such a continuous read function is called a "Multi-Sector Read Operation".

If a TC or an implied TC (FIFO overrun/underrun) is received, the FDC will stop sending data but continue to read data from the current sector and check the CRC bytes until the end of the sector is reached and the READ operation is completed.

The sector size is determined by the N parameter value as calculated in the equation below:

$$\text{Sector Size} = 2^{(7+N \text{ value})} \text{ bytes.}$$

The DTL parameter determines the number of bytes to be transferred. Therefore, if N = 00h, setting the sector size to 128 and the DTL parameter value is less than this, the remaining bytes will be read and checked for CRC errors by the FDC. If this occurs in a WRITE operation, the remaining bytes will be filled with 0. If the sector size is not 128 (N > 00h), DTL should be set to FFh.

In addition to performing Multi-Sector Read operation, the FDC can also perform Multi-Track Read operation. When the MT parameter is set, the FDC can read both sides of a disk automatically.

The combination of N and MT parameter values determines the amount of data that can be transferred during either type of READ operation. Table 9-17 shows the maximum data transfer capacity and the final sector the FDC reads based on these parameters.

Table 9-17. Effects of MT and N Bits

MT	N	Maximum Data Transfer Capacity	Final Sector Read from Disk
0	1	256 X 26 = 6656	26 on side 0 or side 1
1	1	256 X 52 = 13312	26 on side 1
0	2	512 X 15 = 7680	15 on side 0 or side 1
1	2	512 X 30 = 15360	15 on side 1
0	3	1024 X 8 = 8192	8 on side 0 or side 1
1	3	1024 X 16 = 16384	16 on side 1

9.7.11.2 Read Deleted Data

The READ DELETED DATA command is the same as the READ DATA command, except that a Deleted Data Address Mark (as opposed to a Data Address Mark) is read at the beginning of the Data Field. This command is typically used to mark a bad sector on a diskette.

9.7.11.3 Read a Track

After receiving a pulse from the INDEX# pin, the READ A TRACK command reads the entire data field from each sector of the track as a continuous block. If any ID or Data Field CRC error is found, the FDC continues to read data from the track and indicates the error at the end. Because the Multi-Track [and Skip] operation[s] is[are] not allowed under this command, the MT and SK bits should be low (0) during the command execution.

This command terminates normally when the number of sectors specified by EOT has not been read. If, however, no ID Address Mark has been found by the second occurrence of the INDEX pulse, the FDC will set the IC code in the ST0 to 01, indicating an abnormal termination, and then finish the command.

9.7.11.4 Write Data

The WRITE DATA command contains nine command bytes that place the FDC into the Write Data mode. Each WRITE operation is initialized by a WRITE DATA command. The FDC locates the sector to be written by reading ID fields and matching the sector address from the command with the information on the diskette. Then the FDC reads the data from the host via the FIFO and writes the data into the sector's data field. Finally, the FDC computes the CRC value, storing it in the CRC field and increments the sector number (stored in the R parameter) by 1. The next data field is written into the next sector in the same manner. Such a continuous write function is called a "Multi-Sector Write Operation".

If a TC or an implied TC (FIFO overrun/underrun) is received, the FDC stops writing data and fills the remaining data fields with 0s. If a check of the CRC value indicates an error in the sector ID Field, the FDC will set the IC code in ST0 to 01 and the DE bit in ST1 to 1, indicating an abnormal termination, and then terminate the WRITE DATA command. The maximum data transfer capacity and the DTL, N, and MT parameters are the same as in the READ DATA command.

9.7.11.5 Write Deleted Data

The WRITE DELETED DATA command is the same as the WRITE DATA command, except that a Deleted Data Address Mark (instead of a Data Address Mark) is written at the beginning of the Data Field. This command is typically used to mark a bad sector on a diskette.

9.7.11.6 Format A Track

The FORMAT A TRACK command is used to format an entire track. Initialized by an INDEX pulse, it writes data to the Gaps, Address Marks, ID fields and Data fields according to the density mode selected (FM or MFM). The Gap and Data field values are controlled by the host-specified values programmed into N, SC, GPL, and D during the Command phase. The Data field is filled with the data byte specified by D. The four data bytes per sector (C, H, R, and N) needed to fill the ID field are supplied by the host. The C, R, H, and N values must be renewed for each new sector of a track. Only the R parameter value must be changed when a sector is formatted, allowing the disk to be formatted with non-sequential sector addresses. These steps are repeated until a new INDEX pulse is received, at which point the FORMAT A TRACK command is terminated.

9.7.11.7 SCAN

The SCAN command allows the data read from the disk to be compared with the data sent from the system. There are following three SCAN commands:

SCAN EQUAL Disk Data = System Data

SCAN HIGH OR EQUAL Disk Data \geq System Data

SCAN LOW OR EQUAL Disk Data \leq System Data

The SCAN command execution continues until the scan condition has been met, or when the EOT has been reached, or if TC is asserted. Read errors on the disk have the same error condition as the READ DATA command. If the SK bit is set, sectors with Deleted Data Address Marks are ignored. If all sectors' read is skipped, the command terminates with the D3 bit of the ST2 being set. The Result phase of the command is shown below:

Table 9-18. SCAN Command Result

Command	Status Register		Condition
	D2	D3	
SCAN EQUAL	0	1	Disk = System
	1	0	Disk ≠ System
SCAN HIGH OR EQUAL	0	1	Disk = System
	0	0	Disk > System
	1	0	Disk < System
SCAN LOW OR EQUAL	0	1	Disk = System
	0	0	Disk < System
	1	0	Disk > System

9.7.11.8 VERIFY

The VERIFY command is used to read logical sectors containing a Normal Data Address Mark from the selected drive without transferring the data to the host. This command acts like a READ DATA command except that no data are transferred to the host. This command is designed for post-format or post write verification. Data are read from the disk as the controller is checking valid Address Marks in the Address and Data Fields. The CRC is computed and checked against the previously stored value. Because no data are transferred to the host, the TC (Terminal Count of DMA) cannot be used to terminate this command. An implicit TC will be issued to the FDC by setting the EC bit. This implicit TC will occur when the SC value has been decremented to 0. This command can also be terminated by clearing the EC bit and when the EOT value is equal to the final sector to be checked.

Table 9-19. VERIFY Command Result

MT	EC	SC/EOT	Termination Result
0	0	SC = DTL EOT ≤ # Sectors per side	No Error
0	0	SC = DTL EOT > # Sectors per side	Abnormal Termination
0	1	SC ≤ # Sectors Remaining AND EOT ≤ # Sectors per side	No Error
0	1	SC > # Sectors Remaining OR EOT > # Sectors per side	Abnormal Termination
1	0	SC = DTL EOT > # Sectors per side	No Error
1	0	SC = DTL EOT > # Sectors per side	Abnormal Termination
1	1	SC ≤ # Sectors Remaining AND EOT ≤ # Sectors per side	No Error
1	1	SC > # Sectors Remaining OR EOT > # Sectors per side	Abnormal Termination

9.7.12 Control Commands

The control commands do not transfer any data. Instead, these commands are used to monitor and manage the data transfer. Three of them, READ ID, RE-CALIBRATE and SEEK, generate an interrupt after completion. It is strongly recommended that a SENSE INTERRUPT STATUS command be issued after these commands to capture their valuable interrupt information. The RE-CALIBRATE, SEEK, and SPECIFY commands do not return any result bytes.

9.7.12.1 READ ID

The READ ID command is used to find the actual recording head position. It stores the first readable ID field value into the FDC registers. If the FDC cannot find an ID Address Mark by the time the second INDEX pulse is received, an abnormal termination will be generated by setting the IC code in the ST0 to 01.

9.7.12.2 Configure

The CONFIGURE command determines some special operation modes of the controller. It doesn't need to be issued if the default values of the controller meet the system requirements.

EIS: Enable Implied Seeks. A SEEK operation is performed before a READ, WRITE, SCAN, or VERIFY command.

0 = Disabled (default).

1 = Enabled.

DFIFO: Disable FIFO.

0 = Enabled.

1 = Disabled (default).

POLL: Disable polling of the drives.

0 = Enabled (default). When enabled, a single interrupt is generated after a reset.

1 = Disabled.

FIFOTH: The FIFO threshold in the execution phase of data transfer commands. They are programmable from 00 to 0F hex (1 byte to 16 bytes). Default to 1 byte.

PRETRK: The Precompensation Start Track Number. They are programmable from track 0 to FF hex (track 0 to track 255). Default to track 0.

9.7.12.3 RE-CALIBRATE

The RE-CALIBRATE command retracts the FDC read/write head to the position of track 0, resetting the value of the PCN counter and checking the TRK0# status. If TRK0# is low, the DIR# pin remains low and step pulses are issued. If TRK0# is high, either or both of SE and EC bits of the ST0 are set high, and the command is terminated. When TRK0# remains low for 79 step pulses, the RE-CALIBRATE command is terminated by setting SE and EC bits of ST0 to high. Consequently, for disks that can accommodate more than 80 tracks, more than one RE-CALIBRATE command are required to retract the head to the physical track 0.

The FDC is in a non-busy state during the Execution phase of this command, making it possible to issue another RE-CALIBRATE command in parallel with the current command.

On power-up, software must issue a RE-CALIBRATE command to properly initialize the FDC and the drives attached.

9.7.12.4 SEEK

The SEEK command controls the FDC read/write head movement from one track to another. The FDC compares the current head position, stored in PCN, with NCN values after each step pulse to determine what direction to move the head if required. The direction of movement is determined below:

PCN < NCN — Step In: Sets DIR# signal to 1 and issues step pulses.

PCN > NCN — Step Out: Sets DIR# signal to 0 and issues step pulses.

PCN = NCN — Terminate the command by setting ST0 SE bit to 1.

The impulse rate of step pulse is controlled by Stepping Rate Time (SRT) bit in the SPECIFY command. The FDC is in a non-busy state during the Execution phase of this command, making it possible to issue another SEEK command in parallel with the current command.

9.7.12.5 RELATIVE SEEK

The RELATIVE SEEK command steps the selected drive in or out in a given number of steps. The DIR bit is used to determine whether to step in or out. RCN (Relative Cylinder Number) is used to determine how many tracks to step the head in or out from the current track. After the step operation is completed, the controller generates an interrupt, but the command has no Result phase. No other commands except the SENSE INTERRUPT STATUS command should be issued while a RELATIVE SEEK command is in progress.

9.7.12.6 DUMPREG

The DUMPREG command is designed for system run-time diagnostics, application software development, and debug. This command has one byte of Command phase and 10 bytes of Result phase, which returns the values of the parameter set in other commands.

9.7.12.7 LOCK

The LOCK command allows the programmer to fully control the FIFO parameters after a hardware reset. If the LOCK bit is set to 1, the parameters of DFIFO, FIFOTHR, and PRETRK in the CONFIGURE command are not affected by a software reset. If the bit is set to 0, those parameters are set to default values after software reset.

9.7.12.8 VERSION

The VERSION command is used to determine which controller to be used. In the Result phase, a value of 90 hex is returned in order to be compatible with the 82077.

9.7.12.9 SENSE INTERRUPT STATUS

The SENSE INTERRUPT STATUS command resets the interrupt signal (IRQ) generated by the FDC, and identifies the cause of the interrupt via the IC code and SE bit of ST0, as shown in Table 9-20.

It may be necessary to generate an interrupt under any of the following conditions:

- Before any Data Transfer or READ ID command
- After SEEK or RE-CALIBRATE commands (no result phase exists)
- When a data transfer is required during an Execution phase in the non-DMA mode

Table 9-20. Interrupt Identification

SE	IC Code	Cause of Interrupt
0	11	Polling
1	00	Normal termination of SEEK or RE-CALIBRATE command
1	01	Abnormal termination of SEEK or RE-CALIBRATE command

9.7.12.10 SENSE DRIVE STATUS

The SENSE DRIVE STATUS command acquires drive status information. It has no Execution phase.

9.7.12.11 SPECIFY

The SPECIFY command sets the initial values for the HUT (Head Unload Time), HLT (Head Load Time), SRT (Step Rate Time), and ND (Non-DMA mode) parameters. The possible values for HUT, SRT, and HLT are shown in the following three tables respectively. The FDC is operated in the DMA or non-DMA mode based on the value specified by the ND parameters.

Table 9-21. HUT Values

Parameter	1 Mbps	500 Kbps	300 Kbps	250 Kbps
0	128	256	426	512
1	8	16	26.7	32
-	-	-	-	-
E	112	224	373	448
F	120	240	400	480

Table 9-22. SRT Values

Parameter	1 Mbps	500 Kbps	300 Kbps	250 Kbps
0	8	16	26.7	32
1	7.5	15	25	30
-	-	-	-	-
E	1	2	3.33	4
F	0.5	1	1.67	2

Table 9-23. HLT Values

Parameter	1 Mbps	500 Kbps	300 Kbps	250 Kbps
00	128	256	426	512
01	1	2	3.33	4
02	2	4	6.7	8
-	-	-	-	-
7E	126	252	420	504
7F	127	254	423	508

9.7.12.12 PERPENDICULAR MODE

The PERPENDICULAR MODE command is used to support the unique READ/WRITE/FORMAT commands of Perpendicular Recording disk drives (4 Mbytes of unformatted capacity). This command configures each of the four logical drives as a perpendicular or conventional disk drive via the DC3-DC0 bits, or with the GAP and WG control bits. Perpendicular Recording drives operate in the "Extra High Density" mode at 1 Mbps, and are downward compatible with 1.44 Mbyte and 720 kbyte drives at 500 Kbps (High Density) and 250 Kbps (Double Density) respectively. This command should be issued during the initialization of the floppy disk controller. Then, when a drive is accessed for a FORMAT A TRACK or WRITE DATA command, the controller adjusts the format or Write Data parameters based on the data rate. If WG and GAP are used and not set to 00, the operation of the FDC is based on the values of GAP and WG. If WG and GAP are set to 00, setting DCn to 1 will set drive n to the Perpendicular mode. DC3-DC0 are unaffected by a software reset, but WG and GAP are both cleared to 0 after a software reset.

Table 9-24. Effects of GAP and WG on FORMAT A TRACK and WRITE DATA Commands

GAP	WG	Mode	Length of GAP2 FORMAT FIELD	Portion of GAP2 Re-Written by WRITE DATA Command
0	0	Conventional	22 bytes	0 bytes
0	1	Perpendicular (500 Kbps)	22 bytes	19 bytes
1	0	Reserved (Conventional)	22 bytes	0 bytes
1	1	Perpendicular (1 Mbps)	41 bytes	38 bytes

Table 9-25. Effects of Drive Mode and Data Rate on FORMAT A TRACK and WRITE DATA Commands

Data Rate	Drive Mode	Length of GAP2 FORMAT FIELD	Portion of GAP2 Re-Written by WRITE DATA Command
250/300/500 Kbps	Conventional	22 bytes	0 bytes
	Perpendicular	22 bytes	19 bytes
1 Mbps	Conventional	22 bytes	0 bytes
	Perpendicular	41 bytes	38 bytes

9.7.12.13 INVALID

The INVALID command indicates when an undefined command is sent to the FDC. The FDC will set bit 6 and bit 7 in the Main Status Register to 1 and terminate the command without issuing an interrupt.

9.7.13 DMA Transfers

DMA transfers are enabled by the SPECIFY command and are initiated by the FDC by activating the LDRQ# cycle during a DATA TRANSFER command. The FIFO is enabled directly by asserting the LPC DMA cycles.

9.7.14 Low Power Mode

When writing a 1 to the bit 6 of the DSR, the controller is set to the low-power mode immediately. All the clock sources including Data Separator, Microcontroller, and Write precompensation unit will be gated. The FDC can be resumed from the low-power state in two ways: one is a software reset via the DOR or DSR, and the other is a read or write to either the Data Register or Main Status Register. The second method is preferred since all internal register values are retained.

9.8 Serial Port (UART) Description

The IT8720F incorporates two enhanced serial ports that perform serial to parallel conversion on received data, and parallel to serial conversion on transmitted data. Each of the serial channels individually contains a programmable baud rate generator which is capable of dividing the input clock by a number ranging from 1 to 65535. The data rate of each serial port can also be programmed from 115.2K baud down to 50 baud. The character options are programmable for 1 start bit; 1, 1.5 or 2 stop bits; even, odd, stick or no parity; and privileged interrupts.

Table 9-26. Serial Channel Registers

Register	DLAB*	Address	READ	WRITE
Data	0	Base + 0h	RBR (Receiver Buffer Register)	TBR (Transmitter Buffer Register)
Control	0	Base + 1h	IER (Interrupt Enable Register)	IER
	x	Base + 2h	IIR (Interrupt Identification Register)	FCR (FIFO Control Register)
	x	Base + 3h	LCR (Line Control Register)	LCR
	x	Base + 4h	MCR (Modem Control Register)	MCR
	1	Base + 0h	DLL (Divisor Latch LSB)	DLL
	1	Base + 1h	DLM (Divisor Latch MSB)	DLM
Status	x	Base + 5h	LSR (Line Status Register)	LSR
	x	Base + 6h	MSR (Modem Status Register)	MSR
	x	Base + 7h	SCR (Scratch Pad Register)	SCR

* DLAB is bit 7 of the Line Control Register.

9.8.1 Data Registers

The TBR and RBR individually hold five to eight data bits. If the transmitted data are less than eight bits, it aligns to the LSB. Either received or transmitted data are buffered by a shift register, and are latched first by a holding register. Bit 0 of any word is first received and transmitted.

(1) Receiver Buffer Register (RBR) (Read only, Address offset=0, DLAB=0)

This register receives and holds the incoming data. It contains a non-accessible shift register which converts the incoming serial data stream into a parallel 8-bit word.

(2) Transmitter Buffer Register (TBR) (Write only, Address offset=0, DLAB=0)

This register holds and transmits the data via a non-accessible shift register, and converts the outgoing parallel data into a serial stream before data transmission.

9.8.2 Control Registers: IER, IIR, FCR, DLL, DLM, LCR and MCR

(1) Interrupt Enable Register (IER) (Read/Write, Address offset=1, DLAB=0)

The IER is used to enable (or disable) four active high interrupts which activate the interrupt outputs with its lower four bits: IER(0), IER(1), IER(2), and IER(3).

Table 9-27. Interrupt Enable Register Description

Bit	Default	Description
7-4	-	Reserved
3	0	Enable Modem Status Interrupt Set this bit high to enable the modem status interrupt when one of the modem status registers changes its bit status.
2	0	Enable Receiver Line Status Interrupt Set this bit high to enable the receiver line status interrupt, which happens when overrun, parity, framing or break occurs.
1	0	Enable Transmitter Holding Register Empty Interrupt Set this bit high to enable the transmitter holding register empty interrupt.
0	0	Enable Received Data Available Interrupt Set this bit high to enable the received data available interrupt and time-out interrupt in the FIFO mode.

(2) Interrupt Identification Register (IIR) (Read only, Address offset=2)

This register facilitates the host CPU to determine the interrupt priority and its source. The priority of four existing interrupt levels is listed below:

1. Receiver Line Status (highest priority)
2. Received Data Ready
3. Transmitter Holding Register Empty
4. Modem Status (lowest priority)

When a privileged interrupt is pending and the type of interrupt is stored in the IIR which is accessed by the Host, the serial channel holds back all interrupts and indicates the pending interrupts with the highest priority to the Host. Any new interrupts will not be acknowledged until the Host access is completed. The contents of the IIR are described in the following table.

Table 9-28. Interrupt Identification Register

FIFO Mode	Interrupt Identification Register			Interrupt Set and Reset Functions				
	Bit 3	Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Control
	0	X	X	1	-	None	None	-
	0	1	1	0	First	Receiver Line Status	OE, PE, FE, or BI	Read LSR
	0	1	0	0	Second	Received Data Available	Received Data Available	Read RBR or FIFO drops below the trigger level
	1	1	0	0	Second	Character Time-out Indication	No characters have been removed from or input to the RCVR FIFO during the last four character times and there is at least one character in it during this time	Read RBR
	0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Read IIR if THRE is the Interrupt Source Write THR
	0	0	0	0	Fourth	Modem Status	CTS#, DSR#, RI#, DCD#	Read MSR

Note: X = Not Defined

IIR(7), IIR(6): Set when FCR(0) = 1.

IIR(5), IIR(4): Always logic 0.

IIR(3): In the non-FIFO mode, this bit is a logic 0. In the FIFO mode, this bit is set along with bit 2 when a time-out Interrupt is pending.

IIR(2), IIR(1): Used to identify the highest priority interrupt pending.

IR(0): Used to indicate a pending interrupt in either a hard-wired prioritized or polled environment with a logic 0 state. In such a case, IIR contents may be used as a pointer that points to the appropriate interrupt service routine.

(3) FIFO Control Register (FCR) (Write Only, Address offset=2)

This register is used to not only enable and clear the FIFO but also set the RCVR FIFO trigger level.

Table 9-29. FIFO Control Register Description

Bit	Default	Description
7-6	-	Receiver Trigger Level Select These bits set the trigger levels for the RCVR FIFO interrupt.
5-4	0	Reserved
3	0	This bit does not affect the serial channel operation. RXRDY and TXRDY functions are not available on this chip.
2	0	Transmitter FIFO Reset This self-clearing bit clears all contents of the XMIT FIFO and resets its related counter to 0 via a logic "1".
1	0	Receiver FIFO Reset Setting this self-clearing bit to a logic 1 clears all contents of the RCVR FIFO and resets its related counter to 0 (except the shift register).
0	0	FIFO Enable XMIT and RCVR FIFOs are enabled when this bit is set high. XMIT and RCVR FIFOs are disabled and cleared respectively when this bit is cleared to low. This bit has to be a logic 1 if data are written to the other bits of the FCR, or they will not be properly programmed. When this register is switched to the non-FIFO mode, all of its contents are cleared.

Table 9-30. Receiver FIFO Trigger Level Encoding

FCR (7)	FCR (6)	RCVR FIFO Trigger Level
0	0	1 byte
0	1	4 bytes
1	0	8 bytes
1	1	14 bytes

(4) Divisor Latches (DLL, DLM) (Read/Write, Address offset=0,1 DLAB=0)

Two 8-bit Divisor Latches (DLL and DLM) store the divisor values in a 16-bit binary format. They are loaded during the initialization to generate a desired baud rate.

(5) Baud Rate Generator (BRG)

Each serial channel contains a programmable BRG which can take any clock input (from DC to 8 MHz) to generate standard ANSI/CCITT bit rates for the channel clocking with an external clock oscillator. The DLL or DLM is a number of 16-bit format, providing the divisor ranging from 1 to 2^{16} to obtain the desired baud rate. The output frequency is 16X data rate.

Table 9-31. Baud Rates Using (24 MHz ÷ 13) Clock

Desired Baud Rate	Divisor Used
50	2304
75	1536
110	1047
134.5	857
150	768
300	384
600	192
1200	96
1800	64
2000	58
2400	48
3600	32
4800	24
7200	16
9600	12
19200	6
38400	3
57600	2
115200	1

(6) Scratch Pad Register (Read/Write, Address offset=7)

This 8-bit register does not control the UART operation in any way. It is intended as a scratch pad register to be used by programmers to temporarily hold general purpose data.

(7) Line Control Register (LCR) (Read/Write, Address offset=3)

LCR controls the format of the data character and supplies the information of the serial line. Its contents are described in the following table.

Table 9-32. Line Control Register Description

Bit	Default	Description
7	0	Divisor Latch Access Bit (DLAB) This bit must be set to high to access the Divisor Latches of the baud rate generator during READ or WRITE operations. It must be set low to access the Data Registers (RBR and TBR) or the Interrupt Enable Register.
6	0	Set Break This bit forces the Serial Output (SOUT) to the spacing state (logic 0) by a logic 1, which will be preserved until a low level resetting LCR(6), enabling the serial port to alert the terminal in a communication system.
5	0	Stick Parity When this bit and LCR(3) are high at the same time, the parity bit is transmitted and then detected by a receiver in an opposite state by LCR(4) to force the parity bit into a known state and to check the parity bit in a known state.
4	0	Even Parity Select When the parity is enabled (LCR(3) = 1), LCR(4) = 0 selects the odd parity and LCR(4) = 1 selects the even parity.
3	0	Parity Enable A parity bit, located between the last data word bit and stop bit, will be generated or checked (transmit or receive data) when LCR(3) is high.
2	0	Number of Stop Bits This bit specifies the number of stop bits in each serial character, as summarized in Table 9-33. Stop Bits Number Encoding.
1-0	00	Word Length Select [1:0] 11: 8 bits 10: 7 bits 01: 6 bits 00: 5 bits

Table 9-33. Stop Bits Number Encoding

LCR (2)	Word Length	No. of Stop Bits
0	-	1
1	5 bits	1.5
1	6 bits	2
1	7 bits	2
1	8 bits	2

Note: The receiver will ignore all stop bits beyond the first, regardless of the number used in transmission.

(8) Modem Control Register (MCR) (Read/Write, Address offset=4)

It controls the interface by the modem or data set (or device emulating a modem).

Table 9-34. Modem Control Register Description

Bit	Default	Description
7-5	-	Reserved
4	0	Internal Loopback This bit provides a loopback feature for diagnostic test of the serial channel when it is set high. Serial Output (SOUT) is set to the Marking State Shift Register output loops back into the Receiver Shift Register. All Modem Control inputs (CTS#, DSR#, RI# and DCD#) are disconnected. The four Modem Control outputs (DTR#, RTS#, OUT1 and OUT2) are internally connected to the four Modem Control inputs, and are forced to inactive high and the transmitted data are immediately received, allowing the processor to verify the transmit and receive data path of the serial channel.
3	0	OUT2 The Output 2 bit enables the serial port interrupt output by a logic 1.
2	0	OUT1 This bit does not have an output pin and can only be read or written by the CPU.
1	0	Request to Send (RTS) This bit controls the Request to Send (RTS#), which is in an inverse logic state with that of MCR(1).
0	0	Data Terminal Ready (DTR) This bit controls the Data Terminal ready (DTR#), which is in an inverse logic state with that of the MCR(0).

9.8.3 Status Registers: LSR and MSR

(1) Line Status Register (LSR) (Read/Write, Address offset=5)

This register provides the status indication and is usually the first register read by the CPU to determine the cause of an interrupt or to poll the status of each serial channel. The contents of the LSR are described below:

Table 9-35. Line Status Register Description

Bit	Default	Description
7	0	Error in Receiver FIFO In the 16450 mode, this bit is always 0. In the FIFO mode, it is set high when there is at least one parity error, framing or break interrupt in the FIFO. This bit is cleared when the CPU reads the LSR if there are no subsequent errors in the FIFO.
6	1	Transmitter Empty This read only bit indicates that the Transmitter Holding Register and Transmitter Shift Register are both empty. Otherwise, this bit is "0" and has the same function as that in the FIFO mode.
5	1	Transmitter Holding Register Empty (THRE) This read only bit indicates that the TBR is empty and is ready to accept a new character for transmission. It is set high when a character is transferred from the THR into the Transmitter Shift Register, causing a priority 3 IIR interrupt which is cleared by a read of IIR. In the FIFO mode, it is set when the XMIT FIFO is empty, and is cleared when at least one byte is written to the XMIT FIFO.

Bit	Default	Description
4	0	Line Break The Break Interrupt (BI) status bit indicates that the last character received is a break character, which is invalid but complete. It includes parity and stop bits. This occurs when the received data input is held in the spacing (logic 0) for longer than a full word transmission time (start bit + data bits + parity + stop bit). When any of these error conditions is detected (LSR(1) to LSR(4)), a Receiver Line Status interrupt (priority 1) will be generated in the IIR, with the IER(2) previously enabled.
3	0	Framing Error (FE) A logic 1 indicates that the stop bit in the received character is not valid. It will be reset low when the CPU reads the contents of the LSR.
2	0	Parity Error (PE) A logic 1 indicates that the received data character does not have the correct even or odd parity, as selected by LCR(4). It will be reset 0 whenever LSR is read by the CPU.
1	0	Overrun Error (OE) A logic 1 indicates that the RBR has been overwritten by the next character before it had been read by the CPU. In the FIFO mode, OE occurs when FIFO is full and the next character has been completely received by the Shift Register. It will be reset when LSR is read by the CPU.
0	0	Data Ready A logic 1 indicates a character has been received by RBR. A logic 0 indicates all the data in RBR or RCVR FIFO have been read.

(2) Modem Status Register (MSR) (Read/Write, Address offset=6)

This 8-bit register indicates the current state of the control lines with modems or the peripheral devices in addition to this current state information. Four of these eight bits MSR(4) - MSR(7) can provide the state change information when the modem control input changes the state. It is reset low when the Host reads MSR.

Table 9-36. Modem Status Register Description

Bit	Default	Description
7	0	Data Carrier Detect (DCD) It indicates the complement status of Data Carrier Detect (DCD#) input. If MCR(4) = 1, MSR(7) is equivalent to OUT2 of MCR.
6	0	Ring Indicator (RI) It indicates the complement status to the RI# input. If MCR(4)=1, MSR(6) is equivalent to OUT1 of MCR.
5	0	Data Set Ready (DSR) It indicates that the modem is ready to provide received data to the serial channel receiver circuitry. If the serial channel is in the Loop mode (MCR(4) = 1), MSR(5) is equivalent to DTR# in the MCR.
4	0	Clear to Send Clear to Send (CTS) It indicates the complement of CTS# input. When the serial channel is in the loop mode (MCR(4)=1), MSR(5) is equivalent to RTS# in the MCR.
3	0	Delta Data Carrier Detect It indicates that the DCD# input state has been changed since being read by the Host last time.

Bit	Default	Description
2	0	Trailing Edge Ring Indicator It indicates that the RI input state to the serial channel has been changed from low to high since being read by the Host last time. The change in a logic 1 does not activate TERI.
1	0	Delta Data Set Ready (DDSR) A logic 1 indicates that the DSR# input state to the serial channel has been changed since being read by the Host last time.
0	0	Delta Clear to Send This bit indicates the CTS# input to the chip has changed state since MSR was read last time.

9.8.4 Reset

The reset of the IT8720F should be held to an idle mode reset high for 500 ns until initialization, which causes the initialization of the transmitter and receiver internal clock counters.

Table 9-37. Reset Control of Registers and Pinout Signals

Register/Signal	Reset Control	Reset Status
Interrupt Enable Register	Reset	All bits Low
Interrupt Identification Register	Reset	Bit 0 is high and bits 1-7 are low
FIFO Control Register	Reset	All bits Low
Line Control Register	Reset	All bits Low
Modem Control Register	Reset	All bits Low
Line Status Register	Reset	Bits 5 and 6 are high, others are low
Modem Status Register	Reset	Bits 0-3 low, bits 4-7 input signals
SOUT1, SOUT2	Reset	High
RTS1#, RTS2#, DTR1#, DTR2#	Reset	High
IRQ of Serial Port	Reset	High Impedance

9.8.5 Programming

Each serial channel of the IT8720F is programmed by control registers, whose contents define the character length, number of stop bits, parity, baud rate and modem interface. Even though the control register can be written in any given order, IER should be the last register written because it controls whether the interrupt is enabled or not. After the port is programmed, these registers still can be updated whenever the port does not transfer data.

9.8.6 Software Reset

This approach allows the serial port to return to a completely known state without a system reset. It is achieved by writing the required data to LCR, DLL, DLM and MCR. LSR and RBR must be read before interrupts are enabled to clear out any residual data or status bits that may be invalid for subsequent operations.

9.8.7 Clock Input Operation

The input frequency of the Serial Channel is 24 MHz ÷ 13, and not exactly 1.8432 MHz.

9.8.8 FIFO Interrupt Mode Operation

(1) RCVR Interrupt

When setting FCR(0)=1 and IER(0)=1, the RCVR FIFO and receiver interrupts are enabled. The RCVR interrupt occurs under the following conditions:

The received data available interrupt will be issued only when FIFO reaches its programmed trigger level. They will be cleared as soon as FIFO drops below its trigger level.

The receiver line status interrupt has higher priority over the received data available interrupt.

The time-out timer will be reset after receiving a new character or after the Host reads RCVR FIFO whenever a time-out interrupt occurs. The timer will be reset when the Host reads one character from RCVR FIFO.

RCVR FIFO time-out Interrupt: By enabling the RCVR FIFO and receiver interrupts, the RCVR FIFO time-out interrupt will occur under the following conditions:

The RCVR FIFO time-out interrupt will occur only if there is at least one character in FIFO whenever the interval between the most recently received serial character and the most recent Host READ from the FIFO is longer than four consecutive character times.

The time-out timer will be reset after receiving a new character or after the Host reads RCVR FIFO whenever a time-out interrupt occurs. The timer will be reset when the Host reads one character from RCVR FIFO.

(2) XMIT Interrupt

By setting FCR(0) and IER(1) to high, the XMIT FIFO and transmitter interrupts are enabled, and the XMIT interrupt occurs under the following conditions:

- a. The transmitter interrupt occurs when the XMIT FIFO is empty, and it will be reset if the THR is written or the IIR is read.
- b. The transmitter FIFO empty indications will be delayed one character time minus the last stop bit time whenever the following condition occurs:

THRE = 1 and there have not been at least two bytes in the transmitter FIFO at the same time since the last THRE = 1. The transmitter interrupt after changing FCR(0) will be immediate if it is enabled. Once the first transmitter interrupt is enabled, the THRE indication is delayed one character time minus the last stop bit time.

The character time-out and RCVR FIFO trigger level interrupts are in the same priority order as the received data available interrupt. The XMIT FIFO empty is in the same priority as the transmitter holding register empty interrupt.

FIFO Polled Mode Operation [FCR(0)=1, and IER(0), IER(1), IER(2), IER(3) or all are 0].

Either or both XMIT and RCVR can be in this operation mode. The operation mode can be programmed by users and is responsible for checking the RCVR and XMIT status via LSR described below:

LSR(7): RCVR FIFO error indication

LSR(6): XMIT FIFO and Shift register empty

LSR(5): The XMIT FIFO empty indication

LSR(4) - LSR(1): Specify that errors have occurred. The character error status is handled in the same way as that in the interrupt mode. The IIR is not affected since IER(2)=0.

LSR(0): High whenever RCVR FIFO contains at least one byte.
No trigger level is reached or time-out condition indicated in the FIFO Polled Mode.

9.9 Parallel Port

The IT8720F incorporates one multi-mode high performance parallel port, which supports the IBM AT, PS/2 compatible bi-directional Standard Parallel Port (SPP), the Enhanced Parallel Port (EPP) and the Extended Capabilities Port (ECP). Please refer to the IT8720F Configuration registers and Configuration Description for information on enabling/disabling, changing the base address of the parallel port, and operation mode selection.

Table 9-38. Parallel Port Connector in Different Modes

Host Connector	Pin No.	SPP	EPP	ECP
1	11	STB#	WRITE#	NStrobe
2-9	12- 19	PD0 - 7	PD0 - 7	PD0 - 7
10	6	ACK#	INTR	nAck
11	5	BUSY	WAIT#	Busy PeriphAck(2)
12	4	PE	(NU) (1)	PError nAckReverse(2)
13	3	SLCT	(NU) (1)	Select
14	10	AFD#	DSTB#	nAutoFd HostAck(2)
15	9	ERR#	(NU) (1)	nFault nPeriphRequest(2)
16	8	INIT#	(NU) (1)	nInit nReverseRequest(2)
17	7	SLIN#	ASTB#	nSelectIn

Note 1: NU: Not used

Note 2: Fast mode

Note 3: For more information, please refer to the IEEE 1284 standard.

9.9.1 SPP and EPP Modes

Table 9-39. Address Map and Bit Map for SPP and EPP Modes

Register	Address	I/O	D0	D1	D2	D3	D4	D5	D6	D7	Mode
Data Port	Base 1+0h	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	SPP/EPP
Status Port	Base 1+1h	R	TMOUT	1	1	ERR#	SLCT	PE	ACK#	BUSY#	SPP/EPP
Control Port	Base 1+2h	R/W	STB	AFD	INIT	SLIN	IRQE	PDDIR	1	1	SPP/EPP
EPP Address Port	Base 1+3h	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP
EPP Data Port0	Base 1+4h	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP
EPP Data Port1	Base 1+5h	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP
EPP Data Port2	Base 1+6h	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP
EPP Data Port3	Base 1+7h	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP

Note 1: The Base address 1 depends on the Logical Device configuration registers of Parallel Port (0X60, 0X61).

(1) Data Port (Base Address 1 + 00h)

This is a bi-directional 8-bit data port. The direction of data flow is determined by bit 5 of the logic state of the control port register. It forwards the direction when the bit is low and reverses the direction when the bit is high.

(2) Status Port (Base Address 1 + 01h)

This is a **read only** register. Writing to this register has no effects. The contents of this register are latched during an IOR cycle.

Bit 7 - BUSY#: Inverse of printer BUSY signal. A logic "0" means that the printer is busy and cannot accept another character. A logic "1" means that it is ready to accept the next character.

Bit 6 - ACK#: Printer acknowledge. A logic "0" means that the printer has received a character and is ready to accept another. A logic "1" means that it is still processing the last character.

Bit 5 - PE: Paper end. A logic "1" indicates the paper end.

Bit 4 - SLCT: Printer selected. A logic "1" means that the printer is on line.

Bit 3 - ERR#: Printer error signal. A logic "0" means an error has been detected.

Bits 2, 1 - Reserved: These bits are always "1" at read.

Bit 0 - TMOU: This bit is valid only in the EPP mode and indicates that a 10-msec time-out has occurred in EPP operation. A logic "0" means no time-out occurs and a logic "1" means that a time-out error has been detected. This bit is cleared by an LRESET# or by writing a logic "1" to it. When the IT8720F is selected to the non-EPP mode (SPP or ECP), this bit is always a logic "1" at read.

(3) Control Port (Base Address 1 + 02h)

This port provides all output signals to control the printer. The register can be read and written.

Bits 6, 7- Reserved: These two bits are always "1" at read.

Bit 5 - PDDIR: Data port direction control. This bit determines the direction of the data port register. Set this bit "0" to output the data port to PD bus, and "1" to input from PD bus.

Bit 4 - IRQE: Interrupt request enable. Setting this bit "1" enables the interrupt requests from the parallel port to the Host. An interrupt request is generated by a "0" to "1" transition of the ACK# signal.

Bit 3 - SLIN: Inverse of SLIN# pin. Setting this bit to "1" selects the printer.

Bit 2 - INIT: Initiate printer. Setting this bit to "0" initializes the printer.

Bit 1 - AFD: Inverse of the AFD# pin. Setting this bit to "1" causes the printer to automatically advance one line after each line is printed.

Bit 0 - STB: Inverse of the STB# pin. This pin controls the data strobe signal to the printer.

(4) EPP Address Port (Base Address 1 + 03h)

The EPP Address Port is only available in the EPP mode. When the Host writes to this port, the contents of D0 -D7 are buffered and output to PD0 - PD7. The leading edge of IOW (Internal signal, active when LPC I/O WRITE cycle is on this address) causes an EPP ADDRESS WRITE cycle. When the Host reads from this port, the contents of PD0 - PD7 are read. The leading edge of IOR (Internal signal, active when LPC I/O READ cycle is on this address) causes an EPP ADDRESS READ cycle.

(5) EPP Data Ports 0-3 (Base Address 1 + 04-07h)

The EPP Data Ports are only available in the EPP mode. When the Host writes to these ports, the contents of D0 - D7 are buffered and output to PD0 - PD7. The leading edge of IOW (Internal signal, active when LPC I/O WRITE cycle is on this address) causes an EPP DATA WRITE cycle. When the Host reads from these ports, the contents of PD0 - PD7 are read. The leading edge of IOR (Internal signal, active when LPC I/O READ cycle is on this address) causes an EPP DATA READ cycle.

9.9.2 EPP Mode Operation

When the parallel port of the IT8720F is set in the EPP mode, the SPP mode is also available. If no EPP Address/Data Port address is decoded (Base address + 03h- 07h), the PD bus is in the SPP mode, and the output signals such as STB#, AFD#, INIT#, and SLIN# are set by the SPP control port. The direction of the data port is controlled by bit 5 of the control port register. There is a 10-msec time required to prevent the system from lockup. The time has elapsed from the beginning of the IOCHRDY (Internal signal: When active, the IT8720F will issue Long Wait in SYNC field) high (EPP READ/WRITE cycle) to WAIT# being de-asserted.

If a time-out occurs, the current EPP READ/WRITE cycle is aborted and a logic "1" will be read in bit 0 of the status port register. The Host must write 0 to bit 0, 1, 3 of the control port register before any EPP READ/WRITE cycle (EPP spec.). The pins STB#, AFD# and SLIN# are controlled by hardware for the hardware handshaking during EPP READ/WRITE cycle.

(1) EPP ADDRESS WRITE

1. The Host writes a byte to the EPP Address Port (Base address + 03h). The chip drives D0 - D7 onto PD0 - PD7.
2. The chip asserts WRITE# (STB#) and ASTB# (SLIN#) after IOW becomes active.
3. The peripheral de-asserts WAIT#, indicating that the chip may begin the termination of this cycle. Then, the chip de-asserts ASTB#, latches the address from D0 - D7 to PD bus, allowing the Host to complete the I/O WRITE cycle.
4. The peripheral asserts WAIT#, indicating that it acknowledges the termination of the cycle. Then, the chip de-asserts WRITE to terminate the cycle.

(2) EPP ADDRESS READ

1. The Host reads a byte from the EPP Address Port. The chip drives PD bus to tri-state for the peripheral to drive.
2. The chip asserts ASTB# after IOR becomes active.
3. The peripheral drives the PD bus valid and de-asserts WAIT#, indicating that the chip may begin the termination of this cycle. Then, the chip de-asserts ASTB#, latches the address from PD bus to D0 -D7, allowing the Host to complete the I/O READ cycle.
4. The peripheral drives the PD bus to tri-state and then asserts WAIT#, indicating that it acknowledges the termination of the cycle.

(3) EPP DATA WRITE

1. The host writes a byte to the EPP Data Port (Base address +04H - 07H). The chip drives D0- D7 onto PD0 -PD7.
2. The chip asserts WRITE# (STB#) and DSTB# (AFD#) after IOW becomes active.
3. The peripheral de-asserts WAIT#, indicating that the chip may begin the termination of this cycle. Then, the chip de-asserts DSTB#, latches the data from D0 - D7 to the PD bus, allowing the Host to complete the I/O WRITE cycle.
4. The peripheral asserts WAIT#, indicating that it acknowledges the termination of the cycle. Then, the chip de-asserts WRITE to terminate the cycle.

(4) EPP DATA READ

1. The Host reads a byte from the EPP DATA Port. The chip drives PD bus to tri-state for the peripheral to drive.
2. The chip asserts DSTB# after IOR becomes active.
3. The peripheral drives PD bus valid and de-asserts WAIT#, indicating that the chip may begin the termination of this cycle. Then, the chip de-asserts DSTB#, latches the data from PD bus to D0 - D7, allowing the host to complete the I/O READ cycle.
4. The peripheral tri-states the PD bus and then asserts WAIT#, indicating that it acknowledges the termination of the cycle.

9.9.3 ECP Mode Operation

This mode is both software and hardware compatible with the existing parallel ports, allowing ECP to be used as a standard LPT port when the ECP mode is not required. It provides an automatic high-burst-bandwidth channel that supports DMA or the ECP mode in both forward and reverse directions. A 16-byte FIFO is implemented in both forward and reverse directions to smooth data flow and enhance the maximum

bandwidth requirement allowed. The port supports automatic handshaking for the standard parallel port to improve compatibility and expedite the mode transfer. It also supports run-length encoded (RLE) decompression in hardware. Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times a byte has been repeated. The IT8720F does not support hardware RLE compression. For the detailed description, please refer to "Extended Capabilities Port Protocol and ISA Interface Standard".

Table 9-40. Bit Map of the ECP Registers

Register	D7	D6	D5	D4	D3	D2	D1	D0
data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
ecpAFifo	Addr/RLE	Address or RLE field						
dcr	nBusy	nAck	PError	Select	nFault	1	1	1
dcr	1	1	PDDIR	IRQE	SelectIn	nIntr	AutoFd	Strobe
cFifo	Parallel Port Data FIFO							
ecpDFifo	ECP Data FIFO							
tFifo	Test FIFO							
cnfgA	0	0	0	1	0	0	0	0
cnfgB	0	intrValue	0	0	0	0	0	0
ecr	mode			nErrIntrEn	dmaEn	ServiceIntr	full	empty

(1) ECP Register Definitions

Table 9-41. ECP Register Definitions

Name	Address	I/O	ECP Mode	Function
data	Base 1 +000H	R/W	000-001	Data Register
ecpAFifo	Base 1 +000H	R/W	011	ECP FIFO (Address)
dcr	Base 1 +001H	R/W	All	Status Register
dcr	Base 1 +002H	R/W	All	Control Register
cFifo	Base 2 +000H	R/W	010	Parallel Port Data FIFO
ecpDFifo	Base 2 +000H	R/W	011	ECP FIFO (DATA)
tFifo	Base 2 +000H	R/W	110	Test FIFO
cnfgA	Base 2 +000H	R	111	Configuration Register A
cnfgB	Base 2 +001H	R/W	111	Configuration Register B
ecr	Base 2 +002H	R/W	All	Extended Control Register

Note 1: The Base address 1 depends on the Logical Device configuration registers of Parallel Port (0X60, 0X61).

Note 2: The Base address 2 depends on the Logical Device configuration registers of Parallel Port (0X62, 0X63).

(2) ECP Mode Descriptions**Table 9-42. ECP Mode Descriptions**

Mode	Description
000	Standard Parallel Port Mode
001	PS/2 Parallel Port Mode
010	Parallel Port FIFO Mode
011	ECP Parallel Port Mode
110	Test Mode
111	Configuration Mode

Note: Please refer to the ECP Register Description for the detailed description of the mode selection.

(3) ECP Pin Descriptions**Table 9-43. ECP Pin Descriptions**

Name	Attribute	Description
nStrobe (HostClk)	O	Used for handshaking with Busy to write data and addresses into the peripheral device
PD0-PD7	I/O	Address or data or RLE data
nAck (PeriphClk)	I	Used for handshaking with nAutoFd to transfer data from the peripheral device to the Host
Busy (PeriphACK)	I	The peripheral uses this signal for flow control in the forward direction (handshaking with nStrobe). In the reverse direction, this signal is used to determine whether a command or data information is present on PD0-PD7.
Perror (nAckReverse)	I	Used to acknowledge nInIt from the peripheral which drives this signal low, allowing the Host to drive the PD bus
Select	I	Printer On-Line Indication
nAutoFd (HostAck)	O	In the reverse direction, this signal is used for handshaking between the nAck and the Host. When it is asserted, a peripheral data byte is requested. In the forward direction, it is used to determine whether a command or data information is present on PD0 - PD7.
nFault (nPeriphRequest)	I	In the forward direction (only), the peripheral is allowed (but not required) to assert this signal (low) to request a reverse transfer while bringing in the ECP mode. The signal provides a mechanism for peer-to-peer communication. It is typically used to generate an interrupt to the Host, which has the ultimate control over the transfer direction.
nInIt (nReverseRequest)	O	The Host may drive this signal low to make the PD bus in the reverse direction. In the ECP mode, the peripheral is permitted to drive the PD bus when nInIt is low, and nSelectIn is high.
NSelectIn (1284 Active)	O	Always inactive (high) in the ECP mode.

(4) Data Port (Base 1+00h, Modes 000 and 001)

Its contents will be cleared by a reset. In a write operation, the contents of the LPC data fields are latched by the Data Register. The contents are then sent without being inverted to PD0-PD7. In a read operation, the contents of data ports are read and sent to the host.

(5) ecpAFifo Port (Address/RLE) (Base 1 +00h, Mode 011)

Any data bytes written to this port are placed in FIFO and tagged as an ECP Address/RLE. The hardware then automatically sends these data to the peripheral. Operation of this port is valid only in the forward direction (dcr(5)=0).

(6) Device Status Register (dsr) (Base 1 +01h, Mode All)

Bit 0, 1 and 2 of this register are not implemented. The states of these bits remain high in an READ operation of the Printer Status Register.

dsr(7): This bit is the inverted level of the Busy input.

dsr(6): This bit is the state of the nAck input.

dsr(5): This bit is the state of the PError input.

dsr(4): This bit is the state of the Select input.

dsr(3): This bit is the state of the nFault input.

dsr(2)-dsr(0): These bits are always 1.

(7) Device Control Register (dcr) (Base 1+02h, Mode All)

Bit 6 and 7 of this register have no function. They are set high during READ operation, and cannot be written. The contents of bit 0-5 will be initialized to 0 when the RESET pin is active.

dcr(7)-dcr(6): These two bits are always high.

dcr(5): Except in mode 000 and 010, setting this bit low means that the PD bus is in output operation; setting it high means that the PD bus is in input operation. This bit will be forced to low in mode 000.

dcr(4): Setting this bit high enables the interrupt request from peripheral to the host due to a rising edge of the nAck input.

dcr(3): It is inverted and output to SelectIn.

dcr(2): It is output to nInit without inversion.

dcr(1): It is inverted and output to nAutoFd.

dcr(0): It is inverted and output to nStrobe.

(8) Parallel Port Data FIFO (cFifo) (Base 2+00h, Mode 010)

Bytes written or DMA transferred from the Host to this FIFO are sent by a hardware handshaking to the peripheral according to the Standard Parallel Port protocol. This operation is only defined for the forward direction.

(9) ECP Data FIFO (ecpDFifo) (Base 2+00h, Mode 011)

When the direction bit dcr(5) is 0, bytes written or DMA transferred from the Host to this FIFO are sent by hardware handshaking to the peripheral according to the ECP parallel port protocol. When dcr(5) is 1, data bytes from the peripheral to this FIFO are read in an automatic hardware handshaking. The Host can receive these bytes by performing READ operations or DMA transfer from this FIFO.

(10) Test FIFO (tFifo) (Base 2+00h, Mode 110)

The host may operate READ/WRITE or DMA transfer to this FIFO in any directions. Data in this FIFO will be displayed on the PD bus without using hardware protocol handshaking. The tFifo will not accept new data after it is full. Making a READ from an empty tFifo causes the last data byte to return.

(11) Configuration Register A (cnfgA) (Base 2+00h, Mode 111)

This **read only** register indicates to the system that interrupts are ISA-Pulses compatible. This is an 8-bit implementation by returning a 10h.

(12) Configuration Register B (cnfgB) (Base 2+01h, Mode 111)

This register is **read only**.

- cnfgB(7): A logic "0" read indicates that the chip does not support hardware RLE compression.
- cnfgB(6): Reserved.
- cnfgB(5)-cnfg(3): A value 000 read indicates that the interrupt must be selected with jumpers.
- cnfgB(2)-cnfg(0): A value 000 read indicates that the DMA channel is set to 8-bit DMA.

(13) Extended Control Register (ecr) (Base 2+02h, Mode All)

This is an ECP function control register.

- ecr(7)-ecr(5): These bits are used for READ/WRITE and mode selection.

Table 9-44. Extended Control Register (ECR) Mode and Description

ECR	Mode and Description
000	Standard Parallel Port Mode The FIFO is reset and the direction bit dcr(5) is always 0 (forward direction) in this mode.
001	PS/2 Parallel Port Mode It is similar to the SPP mode, except that the dcr(5) is read/write . When dcr(5) is 1, the PD bus is tri-state. Reading the data port returns the value on the PD bus instead of the value of the data register.
010	Parallel Port Data FIFO Mode This mode is similar to the 000 mode, except that the Host writes or DMA transfers the data bytes to FIFO. The FIFO data are then transmitted to the peripheral using the standard parallel port protocol automatically. This mode is only valid in the forward direction (dcr(5)=0).
011	ECP Parallel Port Mode In the forward direction, bytes in the ecpDFifo and ecpAFifo are placed in a single FIFO and automatically transmitted to the peripheral under the ECP protocol. In the reverse direction, bytes are transmitted to the ecpDFifo from the ECP port.
100, 101	Reserved, undefined
110	Test Mode In this mode, FIFO may be read from or written to, but it cannot be sent to the peripheral.
111	Configuration Mode In this mode, the cnfgA and cnfgB registers are accessible at 0x400 and 0x401.

ecr(4): nErrIntrEn, READ/WRITE, Valid in ECP(011) Mode

- 1: Disables the interrupt generated on the asserting edge of the nFault input.
- 0: Enables the interrupt pulse on the asserting edge of the nFault. An interrupt pulse will be generated if nFault is asserted or if this bit is written from 1 to 0 in the low-level nFault.

ecr(3): dmaEn, READ/WRITE

- 1: Enables DMA. DMA is started when serviceIntr (ecr(2)) is 0.
- 0: Disables DMA unconditionally.

ecr(2): ServiceIntr, READ/WRITE

- 1: Disables DMA and all service interrupts.
- 0: Enables the service interrupts. This bit will be set to "1" by hardware when one of the three service interrupts occurs.

Writing "1" to this bit will not generate an interrupt.

Case 1: dmaEn=1

During DMA, this bit will be set to 1 (a service interrupt generated) if the terminal count is reached.

Case 2: dmaEn=0, dcr(5)=0

This bit is set to 1 (a service interrupt generated) whenever there is writeIntrThreshold or more bytes space free in FIFO.

Case 3: dmaEn=0, dcr(5)=1

This bit is set to 1 (a service interrupt generated) whenever there is readIntrThreshold or more valid bytes to be read from FIFO.

ecr(1): full, **read only**

1: FIFO is full and cannot accept another byte.

0: FIFO has at least one free data byte space.

ecr(0): empty, **read only**

1: FIFO is empty.

0: FIFO contains at least one data byte.

(14) Mode Switching Operation

In programmed I/O control (mode 000 or 001), P1284 negotiation and all other tasks that happen before data transmission are software-controlled. Setting the mode to 011 or 010 will cause the hardware to perform an automatic control-line handshaking, transferring information between the FIFO and the ECP port.

Mode 000 or 001 may be immediately switched to any other modes. To change the direction, the mode must first be set to 001.

In the extended forward mode, FIFO must be cleared and all the signals must be de-asserted before returning to mode 000 or 001. In the ECP reverse mode, all data must be read from FIFO before returning to mode 000 or 001. Usually, unneeded data are accumulated during ECP reverse handshaking when the mode is changed during a data transfer. Under such condition, nAutoFd will be de-asserted regardless of the transfer state. To avoid bugs during handshaking signals, these guidelines must be followed.

(15) Software Operation (ECP)

Before ECP operation can be started, it is necessary for the Host to switch the mode to 000 first in order to negotiate with the parallel port. During this process, the Host determines whether the peripheral supports the ECP protocol.

After this negotiation is completed, the mode is set to 011 (ECP). To enable the drivers, the direction must be set to 0. Both strobe and autoFd are set to 0, causing nStrobe and nAutoFd signals to be de-asserted.

All FIFO data transfer is PWord wide and PWord aligned. Permitted only in the forward direction, Address/RLE transfers are byte-wide. The ECP Address/RLE bytes may be automatically sent by writing to the ecpAFifo. Similarly, data PWords may be automatically sent via the ecpDFifo.

To change the direction, the Host has to switch the mode to 001. It then negotiates either the forward or reverse channel, sets the direction to 1 or 0, and finally switches the mode to 001. If the direction is set to 1, hardware performs the handshaking for each ECP data byte read, and then tries to fill FIFO. At this time, PWords may be read from the ecpDFifo while it retains data. It is also possible to perform the ECP transfer by handshaking with individual bytes under programmed control in mode 001 or 000 even though this is a comparatively time-consuming approach.

(16) Hardware Operation (DMA)

The Standard PC DMA protocol (through LDRQ#) is followed. As in the programmed I/O case, software sets the direction and state. Next, the desired count and memory addresses are programmed into the DMA controller. The dmaEn is set to 1, and the serviceIntr is set to 0. To complete the process, the DMA channel with the DMA controller is unmasked. The contents of FIFO are emptied or filled by DMA using the right mode and direction.

DMA is always transferred to or from FIFO located at 0 x 400. By generating an interrupt and asserting a `serviceIntr`, DMA is disabled when the DMA controller reaches the terminal count. By not asserting `LDRQ#` for more than 32 consecutive DMA cycles, blocking of refresh requests is eliminated.

When it is necessary to disable a DMA while performing transfer, the host DMA controller is disabled, then `serviceIntr` is set to 1, and next `dmaEn` is set to 0. If the contents of FIFO are empty or full, DMA will be started again. This is first done by enabling the host DMA controller, and then setting `dmaEn` to 1. Finally, `serviceIntr` is set to 0. Upon completion of a DMA transfer in the forward direction, the software program must wait until the contents of FIFO are empty and the busy line is low, ensuring that all data successfully reach the peripheral device.

(17) Interrupt

It is necessary to generate an interrupt when any of the following states is reached.

1. `serviceIntr = 0`, `dmaEn = 0`, `direction = 0`, and the number of PWords in FIFO is greater than or equal to `writelIntrThreshold`.
2. `serviceIntr = 0`, `dmaEn = 0`, `direction = 1`, and the number of PWords in FIFO is greater than or equal to `readIntrThreshold`.
3. `serviceIntr = 0`, `dmaEn = 1`, and DMA reaches the terminal count.
4. `nErrIntrEn = 0` and `nFault` goes from high to low or when `nErrIntrEn` is set from 1 to 0 and `nFault` is asserted.
5. `ackIntEn = 1`. In current implementations of using existing parallel ports, the interrupt generated may be either edge or level trigger type.

(18) Interrupt-driven Programmed I/O

It is also possible to use an interrupt-driven programmed I/O to execute either ECP or parallel port FIFOs. An interrupt will occur in the forward direction when `serviceIntr` is 0 and the number of free PWords in FIFO is equal to or greater than `writelIntrThreshold`. If either of these conditions is not met, it may be filled with `writelIntrThreshold` PWords. An interrupt will occur in the reverse direction when `serviceIntr` is 0 and the number of available PWords in the FIFO is equal to `readIntrThreshold`. If it is full, FIFO can be completely emptied in a single burst. If it is not full, only a number of PWords equal to `readIntrThreshold` may be read from FIFO in a single burst. In the test mode, software can determine the values of `writelIntrThreshold`, `readIntrThreshold`, and FIFO depth while accessing FIFO.

Any PC LPC bus implementation that is adjusted to expedite DMA or I/O transfer must ensure that the bandwidth on ISA is maintained on the interface. Although the LPC (even PCI) bus of PC cannot be directly controlled, the interface bandwidth of ECP port can be constrained to perform at the optimum speed.

(19) Standard Parallel Port

In the forward direction with DMA, the standard parallel port is run at or close to the permitted peak bandwidth of 500 KB/sec. The state machine does not examine `nAck`, but just begins the next DMA based on the Busy signal.

9.10 Keyboard Controller (KBC)

The keyboard controller is implemented using an 8-bit microcontroller that is capable of executing the 8042 instruction set. For general information, please refer to the description of the 8042 in the 8-bit controller handbook. In addition, the microcontroller can enter the power-down mode by executing two types of power-down instructions.

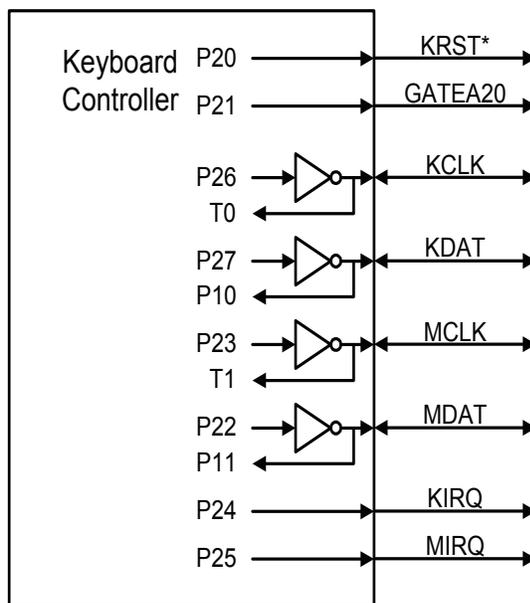


Figure 9-7. Keyboard and Mouse Interface

9.10.1 Host Interface

The keyboard controller interfaces with the system through the 8042 style host interface. The following table shows how the interface decodes the control signals.

Table 9-45. Data Register READ/WRITE Controls

Host Address ^{Note}	R/W*	Function
60h	R	READ DATA
60h	W	WRITE DATA, (Clear F1)
64h	R	READ Status
64h	W	WRITE Command, (Set F1)

Note: These are the default values of LDN5, 60h and 61h (DATA); LDN5, 62h and 63h (Command). All these registers are programmable.

READ DATA: This is an 8-bit **read only** register. When read, the KIRQ output is cleared and OBF flag in the status register is cleared.

WRITE DATA: This is an 8-bit **write only** register. When written, the F1 flag of the Status register is cleared and the IBF bit is set.

READ Status: This is an 8-bit **read only** register. Refer to the description of the Status register for more information.

WRITE Command: This is an 8-bit **write only** register. When written, both F1 and IBF flags of the Status register are set.

9.10.2 Data Registers and Status Register

The keyboard controller provides two data registers, one is DBIN for data input, and the other is DBOU for data output. Both are 8-bit wide. A write (microcontroller) to the DBOU will load Keyboard Data Read Buffer, set OBF flag and set the KIRQ output. A read (microcontroller) of DBIN will read the data from the Keyboard Data or Command Write Buffer and clear the IBF flag.

The status register holds information concerning the status of the data registers, the internal flags, and some user-defined status bits. Please refer to Table 9-46. Status Register below. The bit 0 OBF is set to “1” when the microcontroller writes data into DBOU, and is cleared when the system initiates DATA READ operation. The bit 1 IBF is set to “1” when the system initiates WRITE operation, and is cleared when the microcontroller executes an “IN A, DBB” instruction. The F0 and F1 flags can be set or reset when the microcontroller executes clear and complement flag instructions. F1 also holds the system WRITE information when the system performs WRITE operation.

Table 9-46. Status Register

7	6	5	4	3	2	1	0
ST7	ST6	ST5	ST4	F1	F0	IBF	OBF

9.10.3 Keyboard and Mouse Interface

KCLK is a keyboard clock pin. Its output is the inversion of pin P26 of the microcontroller, and the input of KCLK is connected to the T0 pin of the microcontroller. KDAT is the keyboard data pin; its output is the inversion of pin P27 of the microcontroller, and the input of KDAT is connected to the P10 of the microcontroller. MCLK is the mouse clock pin. Its output is the inversion of pin P23 of the microcontroller, and the input of MCLK is connected to the T1 pin of the microcontroller. MDAT is the mouse data pin. Its output is the inversion of pin P22 of the microcontroller, and the input of MDAT is connected to the P11 of the microcontroller. KRST# is pin P20 of the microcontroller. GATEA20 is the pin P21 of the microcontroller. These two pins are used as software-controlled or user defined outputs. External pull-ups may be required for these pins.

9.10.4 KIRQ and MIRQ

KIRQ is the interrupt request for the keyboard (Default IRQ1), and MIRQ is the interrupt request for the mouse (Default IRQ12). KIRQ is internally connected to P24 pin of the microcontroller, and MIRQ is internally connected to pin P25 of the microcontroller.

9.11 Consumer Remote Control (TV Remote) IR (CIR)

9.11.1 Overview

CIR is used in the consumer remote control equipment, and is a programmable amplitude shift keyed (ASK) serial communication protocol. By adjusting frequencies, baud rate divisors and sensitivity ranges, the CIR registers are able to support the popular protocols such as RC-5, NEC, and RECS-80. Software driver programming can support new protocols.

9.11.2 Features

- Supports 30 kHz – 57 kHz (low frequency) or 400 kHz – 500 kHz (high frequency) carrier transmission
- Baud rate up to 115200 BPS (high frequency)
- Demodulation optional
- Supports transmission run-length encoding and deferral functions
- 32-byte FIFO for data transmission or data reception

9.11.3 Block Diagram

CIR consists of two parts, transmitter and receiver. As for the transmitter part, it is responsible for transmitting data to FIFO, processing FIFO data by serialization and modulation and sending out data through the LED device. As for the receiver part, it is responsible for receiving data, processing data by demodulation and deserialization and storing data in the Receiver FIFO.

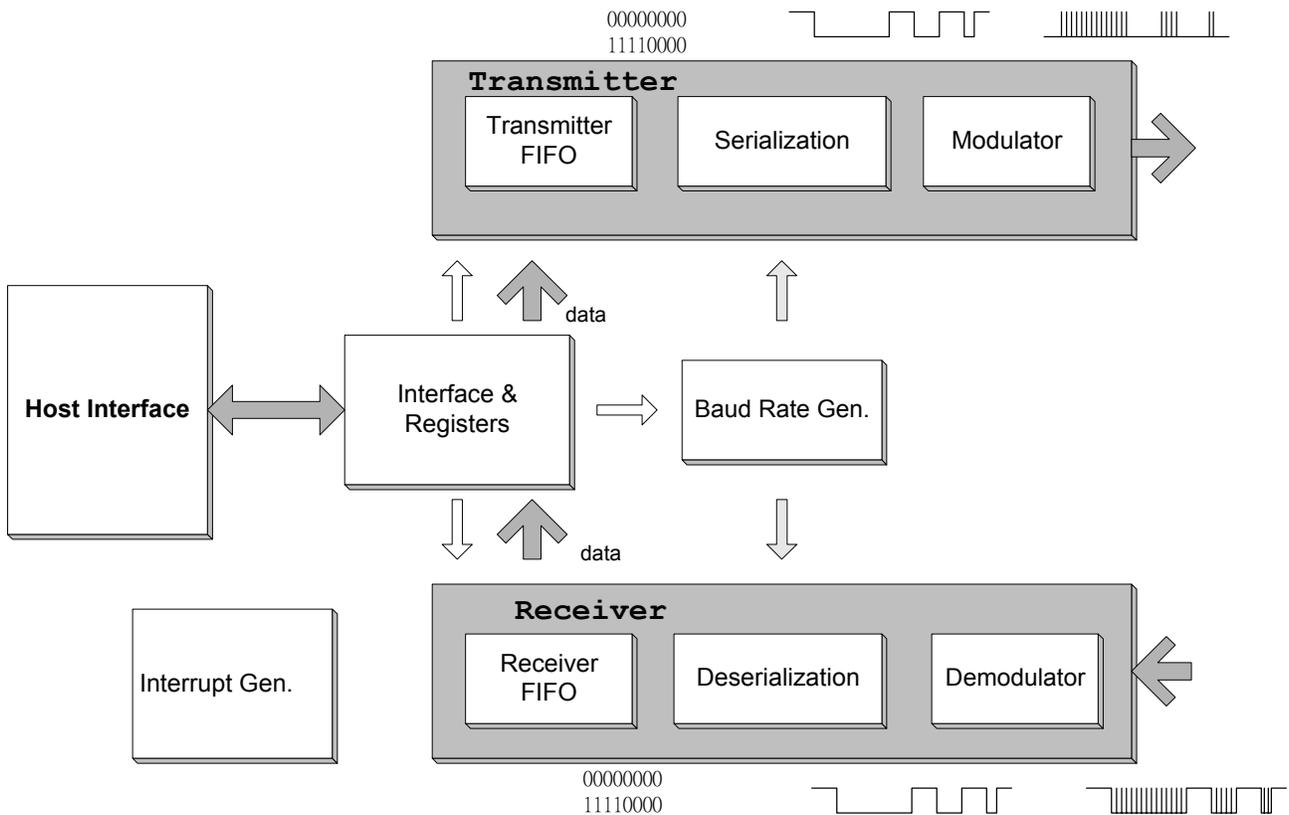


Figure 9-8. CIR Block Diagram

9.11.4 Transmit Operation

The data written to the Transmitter FIFO will be exactly serialized from LSB to MSB, modulated with the carrier frequency and sent to the CIRTX output. The data are either in bit-string format or run-length decode.

Before the data transmission can be started, code byte write operation must be performed to the Transmitter FIFO DR. The bit TXRLE in the TCR1 should be set to “1” before the run-length decode data can be written into the Transmitter FIFO. Setting TXENDF in the TCR1 will enable the data transmission deferral, and avoid the transmitter FIFO underrun. The bit width of the serialized bit string is determined by the value programmed in the baud rate divisor registers, BDLR and BDHR. When the two bits, HCFS and CFQ[4:0], are set, either the high-speed or low-speed carrier range is selected, and the corresponding carrier frequency will also be determined. Bit TXMPM[1:0] and TXMPW[2:0] specify the pulse numbers in a bit width and the required duty cycles of the carrier pulse according to the communication protocol. Only a logic “0” can activate the Transmitter LED in the format of a series of modulating pulses.

9.11.5 Receive Operation

The Receiver function will be enabled if bit RXEN in RCR is set to “1”. Either demodulated or modulated RX# signal is loaded into Receiver FIFO, and bit RXEND in RCR determines whether the demodulation logic should be used or not. It determines the baud rate by programming the baud rate divisor registers BDLR and BDHR, and the carrier frequency by programming bit HCFS and CFQ[4:0]. Set RDWOS to “0” to sync. Bit RXACT in RCR is set to “1” when the serial data or the selected carrier is incoming, and the sampled data will then be kept in Receiver FIFO. Write “1” to bit RXACT to stop the Receiver operation; “0” to bit RXEN to disable the Receiver.

9.11.6 Register Descriptions and Address

Table 9-47. List of CIR Registers

Register Name	R/W	Address	Default
CIR Data Register (DR)	R/W	Base + 0h	FFh
CIR Interrupt Enable Register (IER)	R/W	Base + 1h	00h
CIR Receiver Control Register (RCR)	R/W	Base + 2h	01h
CIR Transmitter Control Register 1 (TCR1)	R/W	Base + 3h	00h
CIR Transmitter Control Register 2 (TCR2)	R/W	Base + 4h	5Ch
CIR Transmitter Status Register (TSR)	R	Base + 5h	00h
CIR Receiver Status Register (RSR)	R	Base + 6h	00h
CIR Baud Rate Divisor Low Byte Register (BDLR)	R/W	Base + 5h	00h
CIR Baud Rate Divisor High Byte Register (BDHR)	R/W	Base + 6h	00h
CIR Interrupt Identification Register (IIR)	R/W	Base + 7h	01h

9.11.6.1 CIR Data Register (DR)

The DR, an 8-bit **read/write** register, is the data port for CIR. Data are transmitted and received through this register.

Address: Base Address + 0h

Bit	R/W	Default	Description
7-0	R/W	FFh	CIR Data Register (DR[7:0]) Writing data to this register causes data to be written to Transmitter FIFO. Reading data from this register causes data to be received from Receiver FIFO.

9.11.6.2 CIR Interrupt Enable Register (IER)

The IER, an 8-bit **read/write** register, is used to enable the CIR interrupt request.

Address: Base Address + 1h

Bit	R/W	Default	Description
7	R/W	0b	Transmitter Data Output Select (TX_sel) This bit is used to select transmitter data output. 0: CIRTX1 (Default) 1: CIRTX2
6	R/W	0b	Receiver Data Input Select (RX_sel) This bit is used to select receiver data input. 0: CIRRX1 (Default) 1: CIRRX2
5	R/W	0b	Rest This bit is with a function of software reset. Writing "1" to this bit resets register DR, IER, TCR1, BDLR, BDHR and IIR. This bit is then cleared to the initial value automatically.
4	R/W	0b	Baud Rate Register Enable Function Enable (BR) This bit is used to control whether the baud rate registers can enable read/write function. Set this bit to "1" to enable the baud rate registers for CIR. Set this bit to "0" to disable the baud rate registers for CIR.
3	R/W	0b	Interrupt Enable Function Control (IEC) This bit is used to control whether the interrupt function can be enabled. Set this bit to "1" to enable the interrupt request for CIR. Set this bit to "0" to disable the interrupt request for CIR.
2	R/W	0b	Receiver FIFO Overrun Interrupt Enable (RFOIE) This bit is used to control Receiver FIFO Overrun Interrupt request. Set this bit to "1" to enable Receiver FIFO Overrun Interrupt request. Set this bit to "0" to disable Receiver FIFO Overrun Interrupt request.
1	R/W	0b	Receiver Data Available Interrupt Enable (RDAIE) This bit is used to enable Receiver Data Available Interrupt request. The Receiver will generate this interrupt when the data available in FIFO exceed the FIFO threshold level. Set this bit to "1" to enable Receiver Data Available Interrupt request. Set this bit to "0" to disable Receiver Data Available Interrupt request.

Bit	R/W	Default	Description
0	R/W	0b	Transmitter Low Data Level Interrupt Enable (TLDLIE) This bit is used to enable Transmitter Low Data Level Interrupt request. The Transmitter will generate this interrupt when the data available in FIFO are less than the FIFO threshold Level. Set this bit to "1" to enable Transmitter Low Data Level Interrupt request. Set this bit to "0" to disable Transmitter Low Data Level Interrupt request.

9.11.6.3 CIR Receiver Control Register (RCR)

The RCR, an 8-bit **read/write** register, is used to control the CIR Receiver.

Address: Base Address + 2h

Bit	R/W	Default	Description
7	R/W	0b	Receiver Data Without Sync. (RDWOS) This bit is used to control the sync. logic for receiving data. Set this bit to "1" to obtain the receiving data without sync. logic. Set this bit to "0" to obtain the receiving data in sync. logic.
6	R/W	0b	High-Speed Carrier Frequency Select (HCFS) This bit is used to select the carrier frequency between the high-speed and low-speed. 0: 30-58 kHz (Default) 1: 400-500 kHz
5	R/W	0b	Receiver Enable (RXEN) This bit is used to enable the Receiver function. Receiver Enable and RXACT will be activated if the selected carrier frequency is received. Set this bit to "1" to enable the Receiver function. Set this bit to "0" to disable the Receiver function.
4	R/W	0b	Receiver Demodulation Enable (RXEND) This bit is used to control the Receiver Demodulation logic. If the Receiver device can not demodulate the correct carrier, set this bit to "1". Set this bit to "1" to enable Receiver Demodulation logic. Set this bit to "0" to disable Receiver Demodulation logic.
3	R/W	0b	Receiver Active (RXACT) This bit is used to control the Receiver operation. This bit is set to "0" when the Receiver is inactive. This bit will be set to "1" when the Receiver detects a pulse (RXEND=0) or pulse-train (RXEND=1) with the correct carrier frequency. The Receiver then starts to sample the input data when Receiver Active is set. Write a "1" to this bit to clear the Receiver Active condition and make the Receiver enter the inactive mode.
2-0	R/W	001b	Receiver Demodulation Carrier Range (RXDCR[2:0]) These three bits are used to set the tolerance of the Receiver. For the detailed demodulation carrier frequency, please refer to Table 9-49. Receiver Demodulation Low Frequency (HCFS = 0) and Table 9-50. Receiver Demodulation High Frequency (HCFS = 1) on page 162 and 163.

9.11.6.4 CIR Transmitter Control Register 1 (TCR1)

The TCR1, an 8-bit **read/write** register, is used to control the Transmitter.

Address: Base Address + 3h

Bit	R/W	Default	Description															
7	R/W	0b	FIFO Clear (FIFOCLR) Writing a "1" to this bit clears FIFO. This bit is then cleared to "0" automatically.															
6	R/W	0b	Internal Loopback Enable (ILE) This bit is used to execute internal loopback for test and must be "0" in normal operation. Set this bit to "0" to disable the Internal Loopback mode. Set this bit to "1" to enable the Internal Loopback mode.															
5-4	R/W	0b	FIFO Threshold Level (FIFOTL) These two bits are used to set the FIFO threshold level. The FIFO length is 32 bytes for TX or RX function (ILE = 0) in normal operation and 16 bytes for both TX and RX in the internal loopback mode (ILE = 1). <table style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th></th> <th>16-Byte Mode</th> <th>32-Byte Mode</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>1</td> <td>1 (Default)</td> </tr> <tr> <td>01</td> <td>3</td> <td>7</td> </tr> <tr> <td>10</td> <td>7</td> <td>17</td> </tr> <tr> <td>11</td> <td>13</td> <td>25</td> </tr> </tbody> </table>		16-Byte Mode	32-Byte Mode	00	1	1 (Default)	01	3	7	10	7	17	11	13	25
	16-Byte Mode	32-Byte Mode																
00	1	1 (Default)																
01	3	7																
10	7	17																
11	13	25																
3	R/W	0b	Transmitter Run Length Enable (TXRLE) This bit controls the Transmitter Run Length encoding/decoding mode, which condenses a series of "1" or "0" into one byte with the bit value stored in bit 7 and number of bits minus 1 in bit 6-0. Set this bit to "1" to enable the Transmitter Run Length mode. Set this bit to "0" to disable the Transmitter Run Length mode.															
2	R/W	0b	Transmitter Deferral (TXENDF) This bit is used to avoid Transmitter underrun condition. When this bit is set to "1", the Transmitter FIFO data will be kept until the transmitter time-out condition occurs, or FIFO reaches full.															
1-0	R/W	0b	Transmitter Modulation Pulse Mode (TXMPM[1:0]) These two bits are used to define the Transmitter modulation pulse mode. TXMPM[1:0] Modulation Pulse Mode C_pls mode (Default): Pulses are generated continuously for the entire logic 0 bit time. 8_pls mode: 8 pulses are generated for each logic 0 bit. 6_pls mode: 6 pulses are generated for each logic 0 bit. 11: Reserved.															

9.11.6.5 CIR Transmitter Control Register (TCR2)

The TCR2, an 8-bit **read/write** register, is used to determine the carrier frequency.

Address: Base Address + 4h

Bit	R/W	Default	Description																											
7-3	R/W	01011b	Carrier Frequency (CFQ[4:0]) These five bits are used to determine the modulation carrier frequency. Please refer to the following table.																											
2-0	R/W	100b	Transmitter Modulation Pulse Width (TXMPW[2:0]) These three bits are used to set the Transmitter Modulation pulse width. The duty cycle of the carrier will be determined according to the settings of the carrier frequency and the selection of Transmitter Modulation pulse width. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>TXMPW[2:0]</th> <th>HCFS = 0</th> <th>HCFS = 1</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>Reserved</td> <td>Reserved</td> </tr> <tr> <td>001</td> <td>Reserved</td> <td>Reserved</td> </tr> <tr> <td>010</td> <td>6 μs</td> <td>0.7 μs</td> </tr> <tr> <td>011</td> <td>7 μs</td> <td>0.8 μs</td> </tr> <tr> <td>100</td> <td>8.7 μs</td> <td>0.9 μs (Default)</td> </tr> <tr> <td>101</td> <td>10.6 μs</td> <td>1.0 μs</td> </tr> <tr> <td>110</td> <td>13.3 μs</td> <td>1.16 μs</td> </tr> <tr> <td>111</td> <td>Reserved</td> <td>Reserved</td> </tr> </tbody> </table>	TXMPW[2:0]	HCFS = 0	HCFS = 1	000	Reserved	Reserved	001	Reserved	Reserved	010	6 μ s	0.7 μ s	011	7 μ s	0.8 μ s	100	8.7 μs	0.9 μs (Default)	101	10.6 μ s	1.0 μ s	110	13.3 μ s	1.16 μ s	111	Reserved	Reserved
TXMPW[2:0]	HCFS = 0	HCFS = 1																												
000	Reserved	Reserved																												
001	Reserved	Reserved																												
010	6 μ s	0.7 μ s																												
011	7 μ s	0.8 μ s																												
100	8.7 μs	0.9 μs (Default)																												
101	10.6 μ s	1.0 μ s																												
110	13.3 μ s	1.16 μ s																												
111	Reserved	Reserved																												

Table 9-48. Modulation Carrier Frequency

CFQ	Low Frequency (HCFS = 0)	High Frequency (HCFS = 1)
00000	27 kHz	-
00010	29 kHz	-
00011	30 kHz	400 kHz
00100	31 kHz	-
00101	32 kHz	-
00110	33 kHz	-
00111	34 kHz	-
01000	35 kHz	450 kHz
01001	36 kHz	-
01010	37 kHz	-
01011	38 kHz (default)	480 kHz (default)
01100	39 kHz	-
01101	40 kHz	500 kHz
01110	41 kHz	-
01111	42 kHz	-
10000	43 kHz	-
10001	44 kHz	-
10010	45 kHz	-
10011	46 kHz	-
10100	47 kHz	-
10101	48 kHz	-
10110	49 kHz	-
10111	50 kHz	-
11000	51 kHz	-
11001	52 kHz	-
11010	53 kHz	-
11011	54 kHz	-
11100	55 kHz	-
11101	56 kHz	-
11110	57 kHz	-
11111	58 kHz	-

Table 9-49. Receiver Demodulation Low Frequency (HCFS = 0)

RXDCR	001		010		011		100		101		110		(Hz)
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
00001	26.25	29.75	24.5	31.5	22.75	33.25	21	35	19.25	36.75	17.5	38.5	28k
00010	27.19	30.81	25.38	32.63	23.56	34.44	21.75	36.25	19.94	38.06	18.13	39.88	29k
00011	28.13	31.88	26.25	33.75	24.38	35.63	22.5	37.5	20.63	39.38	18.75	41.25	30k
00100	29.06	32.94	27.13	34.88	25.19	36.81	23.25	38.75	21.31	40.69	19.38	42.63	31k
00101	30	34	28	36	26	38	24	40	22	42	20	44	32k
00110	30.94	35.06	28.88	37.13	26.81	39.19	24.75	41.25	22.69	43.31	20.63	45.38	33k
00111	31.88	36.13	29.75	38.25	27.63	40.38	25.5	42.5	23.38	44.63	21.25	46.75	34k
01000	32.81	37.19	30.63	39.38	28.44	41.56	26.25	43.75	24.06	45.94	21.88	48.13	35k
01001	33.75	38.25	31.5	40.5	29.25	42.75	27	45	24.75	47.25	22.5	49.5	36k
01010	34.69	39.31	32.38	41.63	30.06	43.94	27.75	46.25	25.44	48.56	23.13	50.88	37k
01011	35.63	40.38	33.25	42.75	30.88	45.13	28.5	47.5	26.13	49.88	23.75	52.25	38k
01100	36.56	41.44	34.13	43.88	31.69	46.31	29.25	48.75	26.81	51.19	24.38	53.63	39k
01101	37.5	42.5	35	45	32.5	47.5	30	50	27.5	52.5	25	55	40k
01110	38.44	43.56	35.88	46.13	33.31	48.69	30.75	51.25	28.19	53.81	25.63	56.38	41k
01111	39.38	44.63	36.75	47.25	34.13	49.88	31.5	52.5	28.88	55.13	26.25	57.75	42k
10000	40.31	45.69	37.63	48.38	34.94	51.06	32.25	53.75	29.56	56.44	26.88	59.13	43k
10001	41.25	46.75	38.5	49.5	35.75	52.25	33	55	30.25	57.75	27.5	60.5	44k
10010	42.19	47.81	39.38	50.63	36.56	53.44	33.75	56.25	30.94	59.06	28.13	61.88	45k
10011	43.13	48.88	40.25	51.75	37.38	54.63	34.5	57.5	31.63	60.38	28.75	63.25	46k
10100	44.06	49.94	41.13	52.88	38.19	55.81	35.25	58.75	32.31	61.69	29.38	64.63	47k
10101	45	51	42	54	39	57	36	60	33	63	30	66	48k
10110	45.94	52.06	42.88	55.13	39.81	58.19	36.75	61.25	33.69	64.31	30.63	67.38	49k
10111	46.88	53.13	43.75	56.25	40.63	59.38	37.5	62.5	34.38	65.63	31.25	68.75	50k
11000	47.81	54.19	44.63	57.38	41.44	60.56	38.25	63.75	35.06	66.94	31.88	70.13	51k
11001	49.18	54.55	46.88	57.69	44.78	61.22	42.86	65.22	41.1	69.77	39.47	75	52k
11010	49.69	56.31	46.38	59.63	43.06	62.94	39.75	66.25	36.44	69.56	33.13	72.88	53k
11011	50.63	57.38	47.25	60.75	43.88	64.13	40.5	67.5	37.13	70.88	33.75	74.25	54k
11100	51.56	58.44	48.13	61.88	44.69	65.31	41.25	68.75	37.81	72.19	34.38	75.63	55k
11101	52.5	59.5	49	63	45.5	66.5	42	70	38.5	73.5	35	77	56k
11110	53.44	60.56	49.88	64.13	46.31	67.69	42.75	71.25	39.19	74.81	35.63	78.38	57k

Table 9-50. Receiver Demodulation High Frequency (HCFS = 1)

RXDCR	001		010		011		100		101		110		
CFQ	Min.	Max.	(Hz)										
00011	375	425	350	450	325	475	300	500	275	525	250	550	400k
01000	421.9	478.1	393.8	506.3	365.6	534.4	337.5	562.5	309.4	590.6	281.3	618.8	450k
01011	450	510	420	540	390	570	360	600	330	630	300	660	480k
01011	468.8	531.3	437.5	562.5	406.3	593.8	375	625	343.8	656.3	312.5	687.5	500k

9.11.6.6 CIR Baud Rate Divisor Low Byte Register (BDLR)

The BDLR, an 8-bit **read/write** register, is used to program the CIR Baud Rate clock.

Address: Base Address + 5h (when BR = 1)

Bit	R/W	Default	Description
7-0	R/W	00h	Baud Rate Divisor Low Byte (BDLR[7:0]) These bits are the low byte of the register used to divide the Baud Rate clock.

9.11.6.7 CIR Baud Rate Divisor High Byte Register (BDHR)

The BDHR, an 8-bit **read/write** register, is used to program the CIR Baud Rate clock.

Address: Base Address + 6h (when BR = 1)

Bit	R/W	Default	Description
7-0	R/W	00h	Baud Rate Divisor High Byte (BDHR[7:0]) These bits are the high byte of the register used to divide the Baud Rate clock.

Baud rate divisor = 115200 / baud rate

Ex1: 2400 bps → 115200 / 2400 = 48 → 48(d) = 0030(h) → BDHR = 00h, BDLR = 30h

Ex2: bit width = 0.565 ms (1770 bps (115200 / 1770 = 65(d) = 0041(h) (BDHR = 00(h), BDLR = 41(h)

9.11.6.8 CIR Transmitter Status Register (TSR)

The TSR, an 8-bit **read only** register, provides the Transmitter FIFO status.

Address: Base Address + 5h

Bit	R/W	Default	Description
7-6	R	-	Reserved
5-0	R	000000b	Transmitter FIFO Byte Count (TXFBC[5:0]) Return the number of bytes left in the Transmitter FIFO.

9.11.6.9 CIR Receiver FIFO Status Register (RSR)

The RSR, an 8-bit **read only** register, provides the Receiver FIFO status.

Address: Base Address + 6h

Bit	R/W	Default	Description
7	R	0b	Receiver FIFO Time-out (RXFTO) This bit will be set to “1” when a Receiver FIFO time-out condition occurs. The conditions required for the occurrence of Receiver FIFO time-out condition include the followings: When at least one byte of data are queued in the Receiver FIFO for more than 64 ms and the receiver has been inactive (RXACT=0) for more than 64 ms.
6	-	-	Reserved
5-0	R	000000b	Receiver FIFO Byte Count (RXFBC) Return the number of bytes left in Receiver FIFO.

9.11.6.10 CIR Interrupt Identification Register (IIR)

The IIR, an 8-bit register, is used to identify the pending interrupts.

Address: Base address + 7h

Bit	R/W	Default	Description
7-3	-	-	Reserved
2-1	R	00b	Interrupt Identification These two bits are used to identify the source of the pending interrupt. IIR[1:0] Interrupt Source 00 No interrupt 01 Transmitter Low Data Level Interrupt 10 Receiver Data Stored Interrupt 11 Receiver FIFO Overrun Interrupt
0	R	1b	Interrupt Pending This bit will be set to “1” while an interrupt is pending.

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10. DC Electrical Characteristics

Absolute Maximum Ratings*

Applied Voltage	-0.5V to 5.5V
Input Voltage (Vi).....	-0.5V to VCC+0.5V
Output Voltage (Vo).....	-0.5V to VCC + 0.3V
Operation Temperature (Topt).....	0°C to +70°C
Storage Temperature	-55°C to +125°C
Power Dissipation	300mW

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (VCC = 5V ± 5%, Ta = 0°C to + 70°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
DO8 Buffer						
V _{OL}	Low Output Voltage	I _{OL} = 8 mA			0.4	V
V _{OH}	High Output Voltage	I _{OH} = -8 mA	2.4			V
DOD8 Buffer						
V _{OL}	Low Output Voltage	I _{OL} = 8 mA			0.4	V
DO16 Buffer						
V _{OL}	Low Output Voltage	I _{OL} = 16 mA			0.4	V
V _{OH}	High Output Voltage	I _{OH} = -16 mA	2.4			V
DO24 Buffer						
V _{OL}	Low Output Voltage	I _{OL} = 24 mA			0.4	V
V _{OH}	High Output Voltage	I _{OH} = -16 mA	2.4			V
DO24L Buffer						
V _{OL}	Low Output Voltage	I _{OL} = 24 mA			0.4	V
V _{OH}	High Output Voltage	I _{OH} = -8 mA	2.4			V
DIO8 Type Buffer						
V _{OL}	Low Output Voltage	I _{OL} = 8 mA			0.4	V
V _{OH}	High Output Voltage	I _{OH} = -8 mA	2.4			V
V _{IL}	Low Input Voltage				0.8	V
V _{IH}	High Input Voltage		2.2			V
I _{IL}	Low Input Leakage	V _{IN} = 0		10		μA
I _{IH}	High Input Leakage	V _{IN} = VCC			-10	μA
I _{OZ}	3-state Leakage				20	μA

DC Electrical Characteristics (VCC = 5V ± 5%, Ta = 0°C to + 70°C)[cont'd]

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
DIOD8 Type Buffer						
V _{OL}	Low Output Voltage	I _{OL} = 8 mA			0.4	V
V _{IL}	Low Input Voltage				0.8	V
V _{IH}	High Input Voltage		2.2			V
I _{IL}	Low Input Leakage	V _{IN} = 0		10		μA
I _{IH}	High Input Leakage	V _{IN} = VCC			-10	μA
I _{OZ}	3-state Leakage				20	μA
DIO16 Type Buffer						
V _{OL}	Low Output Voltage	I _{OL} = 16 mA			0.4	V
V _{OH}	High Output Voltage	I _{OH} = -16 mA	2.4			V
V _{IL}	Low Input Voltage				0.8	V
V _{IH}	High Input Voltage		2.2			V
I _{IL}	Low Input Leakage	V _{IN} = 0		10		μA
I _{IH}	High Input Leakage	V _{IN} = VCC			-10	μA
I _{OZ}	3-state Leakage				20	μA
DIOD16 Type Buffer						
V _{OL}	Low Output Voltage	I _{OL} = 16 mA			0.4	V
V _{IL}	Low Input Voltage				0.8	V
V _{IH}	High Input Voltage		2.2			V
I _{IL}	Low Input Leakage	V _{IN} = 0		10		μA
I _{IH}	High Input Leakage	V _{IN} = VCC			-10	μA
I _{OZ}	3-state Leakage				20	μA
DIO24 Type Buffer						
V _{OL}	Low Output Voltage	I _{OL} = 24 mA			0.4	V
V _{OH}	High Output Voltage	I _{OH} = -16 mA	2.4			V
V _{IL}	Low Input Voltage				0.8	V
V _{IH}	High Input Voltage		2.2			V
I _{IL}	Low Input Leakage	V _{IN} = 0		10		μA
I _{IH}	High Input Leakage	V _{IN} = VCC			-10	μA
I _{OZ}	3-state Leakage				20	μA
DI Type Buffer						
V _{IL}	Low Input Voltage				0.8	V
V _{IH}	High Input Voltage		2.2			V
I _{IL}	Low Input Leakage	V _{IN} = 0		10		μA
I _{IH}	High Input Leakage	V _{IN} = VCC			-10	μA

11. AC Characteristics (VCC = 5V ± 5%, Ta = 0°C to + 70°C)

11.1 Clock Input Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t ₁	Clock High Pulse Width when CLKIN=48 MHz ¹	8			nsec
t ₂	Clock Low Pulse Width when CLKIN=48 MHz ¹	8			nsec
t ₃	Clock Period when CLKIN=48 MHz ¹	20	21	22	nsec
t ₄	Clock High Pulse Width when CLKIN=24 MHz ¹	18			nsec
t ₅	Clock Low Pulse Width when CLKIN=24 MHz ¹	18			nsec
t ₆	Clock Period when CLKIN=24 MHz ¹	40	42	44	nsec

Not tested. Guaranteed by design.

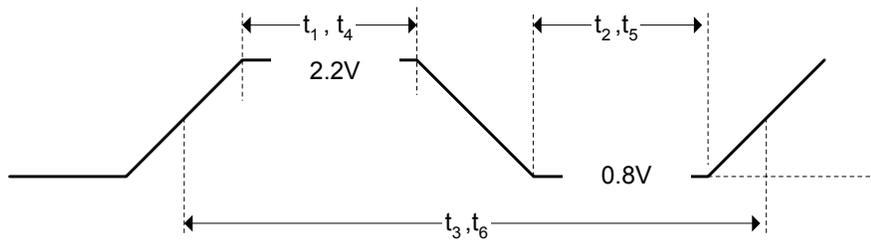


Figure 11-1. Clock Input Timings

11.2 LCLK (PCICLK) and LRESET Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	LCLK Cycle Time	28			nsec
t_2	LCLK High Time	11			nsec
t_3	LCLK Low Time	11			nsec
t_4	LRESET# Low Pulse Width	1.5			μ sec

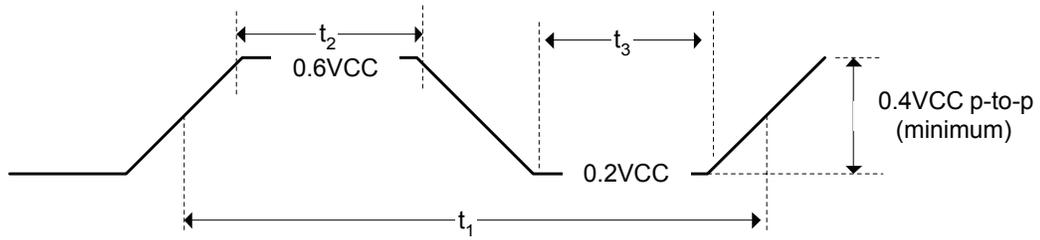


Figure 11-2. LCLK (PCICLK) and LRESET Timings

11.3 LPC and SERIRQ Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	Float to Active Delay	3			nsec
t_2	Output Valid Delay			12	nsec
t_3	Active to Float Delay			6	nsec
t_4	Input Setup Time	9			nsec
t_5	Input Hold Time	3			nsec

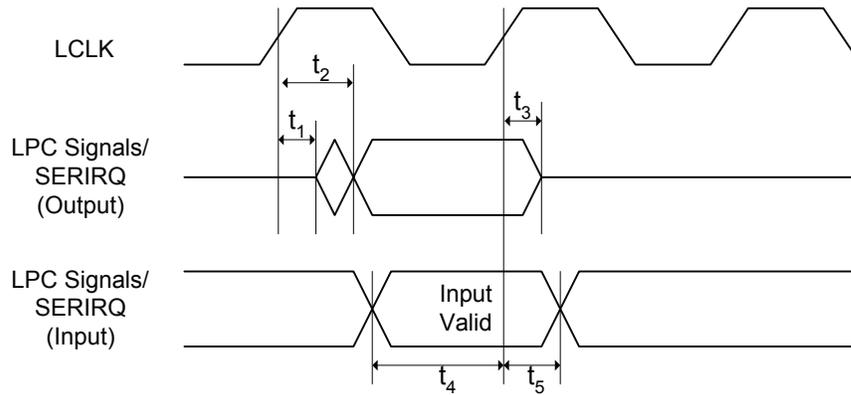


Figure 11-3. LPC and SERIRQ Timings

11.4 Serial Port, ASKIR, SIR and Consumer Remote Control Timings

Symbol	Parameter	Conditions	Min.	Max.	Unit
t_1	Single Bit Time in Serial Port and ASKIR	Transmitter	$t_{BTN} - 25$ ^{Note1}	$t_{BTN} + 25$	nsec
		Receiver	$t_{BTN} - 2\%$	$t_{BTN} + 2\%$	nsec
t_2	Modulation Signal Pulse Width in ASKIR	Transmitter	950	1050	nsec
		Receiver	500		nsec
t_3	Modulation Signal Period in ASKIR	Transmitter	1975	2025	nsec
		Receiver	$2000 \times (23/24)$	$2000 \times (25/24)$	nsec
t_4	SIR Signal Pulse Width	Transmitter, Variable	$(3/16) \times t_{BTN} - 25$	$(3/16) \times t_{BTN} + 25$	nsec
		Transmitter, Fixed	1.48	1.78	μ sec
		Receiver	1		μ sec

Note 1: t_{BTN} is the nominal bit time in Serial Port, ASKIR, and SIR. It is determined by the setting on the Baud Rate Divisor registers.

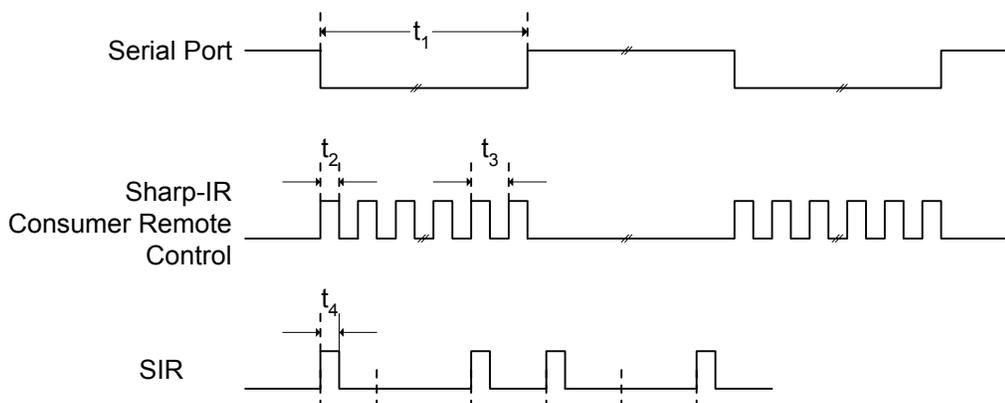


Figure 11-4. Serial Port, ASKIR, SIR and Consumer Remote Control Timings

11.5 Modem Control Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	Float to active delay			40	nsec

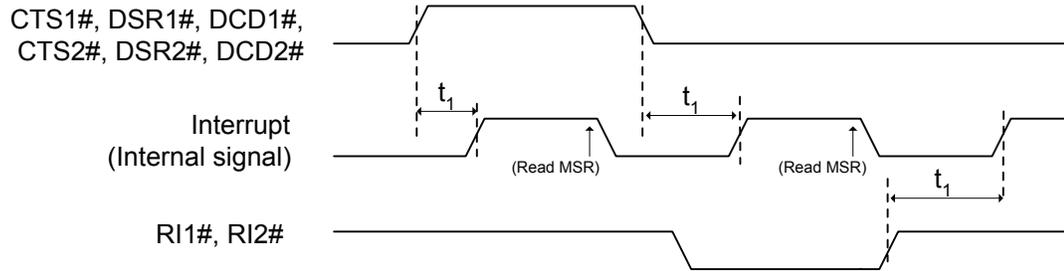


Figure 11-5. Modem Control Timings

11.6 Floppy Disk Drive Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	DIR# active to STEP# low		$4X t_{mclk}$ ^{Note1}		nsec
t_2	STEP# active time (low)		$24X t_{mclk}$		nsec
t_3	DIR# hold time after STEP#		t_{SRT} ^{Note2}		msec
t_4	STEP# cycle time		t_{SRT}		msec
t_5	INDEX# low pulse width	$2X t_{mclk}$			nsec
t_6	RDATA# low pulse width	40			nsec
t_7	WDATA# low pulse width		$1X t_{mclk}$		nsec

Note 1: t_{mclk} is the cycle of main clock for the microcontroller of FDC. $t_{mclk} = 8M/ 4M/ 2.4M/ 2M$ for 1M/ 500K/ 300K/ 250 Kbps transfer rates respectively.

Note 2: t_{SRT} is the cycle of the Step Rate Time. Please refer to the functional description of the SPECIFY command of the FDC.

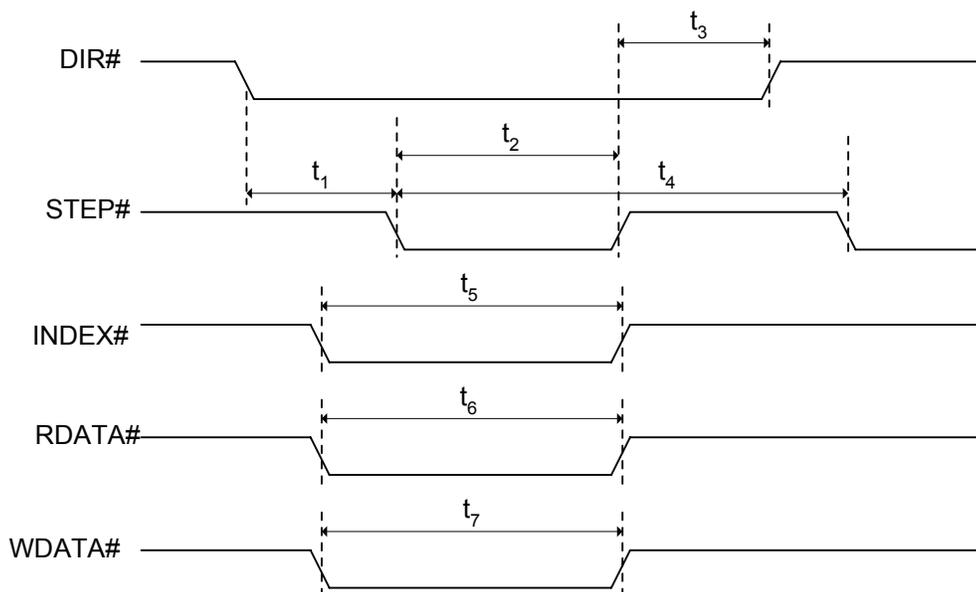


Figure 11-6. Floppy Disk Drive Timings

11.7 EPP Address or Data Write Cycle Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	WRITE# asserted to PD[7:0] valid			50	nsec
t_2	ASTB# or DSTB# asserted to WAIT# de-asserted	0		10	nsec
t_3	WAIT# de-asserted to ASTB# or DSTB# de-asserted	65		135	nsec
t_4	ASTB# or DSTB# de-asserted to WAIT# asserted	0			nsec
t_5	WAIT# asserted to WRITE# de-asserted	65			nsec
t_6	PD[7:0] invalid after WRITE# de-asserted	0			nsec

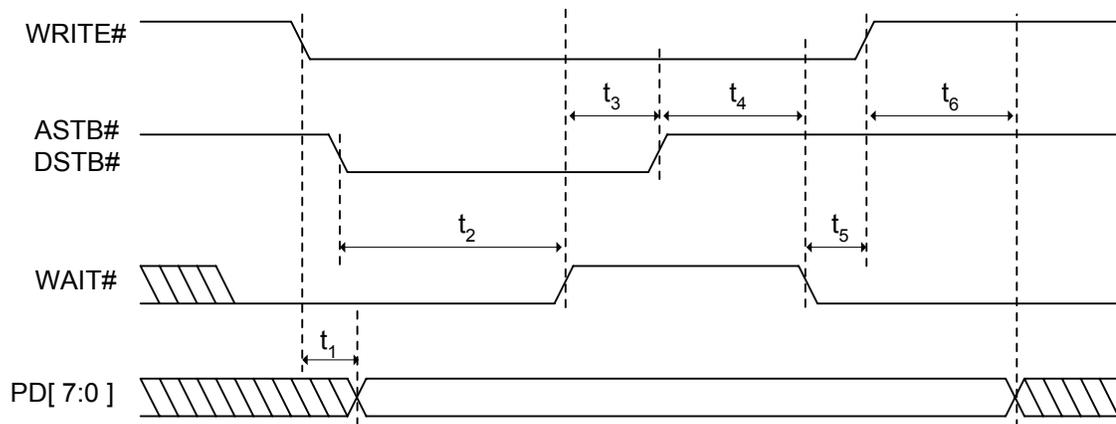


Figure 11-7. EPP Address or Data Write Cycle Timings

11.8 Keyboard/Mouse Receive/Send Data Timing Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	Time form DATA transition to falling edge of CLK (Receive)	5		25	μ sec
t_2	Time form rising edge of CLK to DATA transition (Receive)	5		T4-5	μ sec
t_3	Duration of CLK inactive (Receive/Send)	30		50	μ sec
t_4	Duration of CLK active (Receive/Send)	30		50	μ sec
t_5	Time to keyboard inhibit after clock 11 to ensure the keyboard device does not start another transmission (Receive)	>0	50		μ sec
t_6	Time from inactive to active CLOCK transition, used to time when the auxiliary device samples DATA (Send)	5		25	μ sec

Note: (1) The system can hold the 'clock' signal inactive to inhibit the next transmission.
 (2) The system raises the 'clock' line to allow the next transmission.

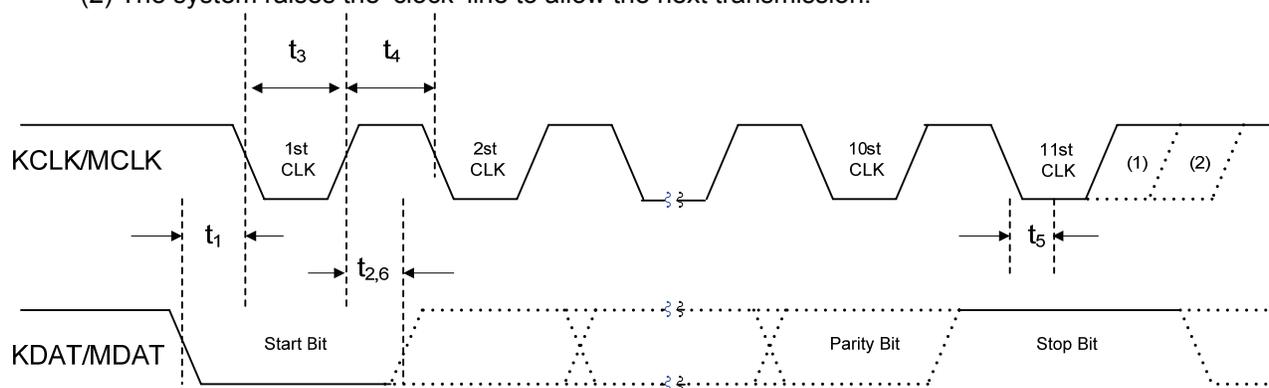


Figure 11-8. Keyboard/Mouse Receive/Send Data Timing

11.9 EPP Address or Data Read Cycle Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	ASTB# or DSTB# asserted to WAIT# de-asserted			10	nsec
t_2	ASTB# or DSTB# asserted to PD[7:0] Hi-Z	0			nsec
t_3	PD[7:0] valid to WAIT# de-asserted	0			nsec
t_4	WAIT# de-asserted to ASTB# or DSTB# de-asserted	65		135	nsec
t_5	ASTB# or DSTB# de-asserted to WAIT# asserted	0			nsec
t_6	PD[7:0] invalid after ASTB# or DSTB# de-asserted	20			nsec

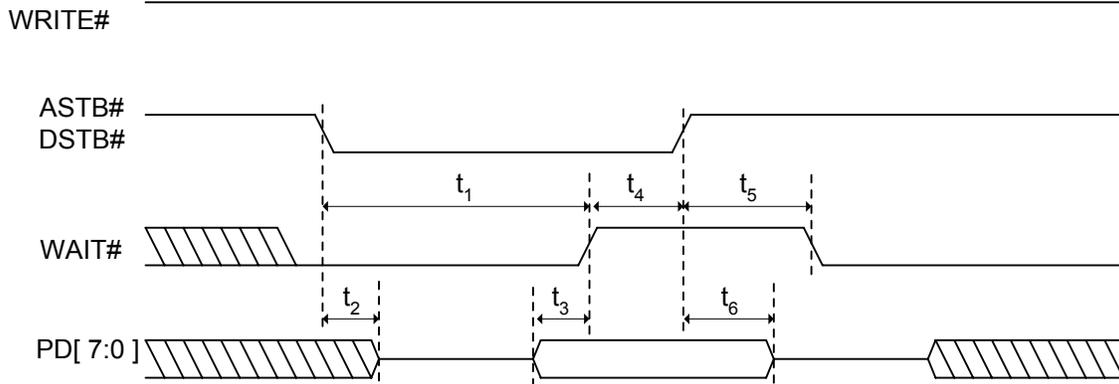


Figure 11-9. EPP Address or Data Read Cycle Timings

11.10 ECP Parallel Port Forward Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	PD[7:0] and nAutoFd valid to nStrobe asserted			50	nsec
t_2	nStrobe asserted to Busy asserted	0			nsec
t_3	Busy asserted to nStrobe de-asserted	70		170	nsec
t_4	nStrobe de-asserted to Busy de-asserted	0			nsec
t_5	Busy de-asserted to PD[7:0] and nAutoFd changed	80		180	nsec
t_6	Busy de-asserted to nStrobe asserted	70		170	nsec

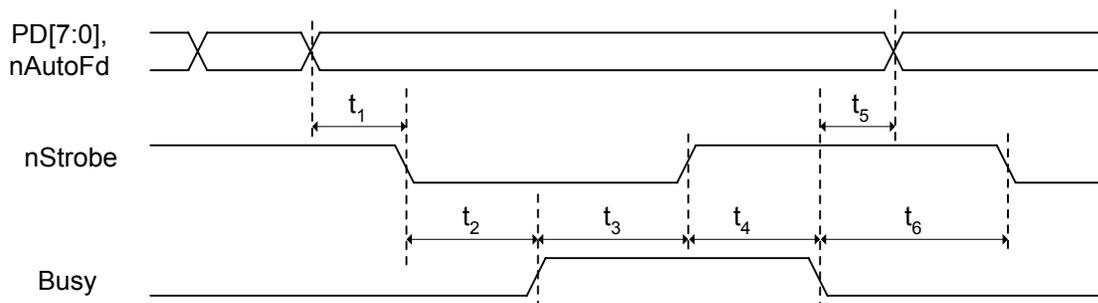


Figure 11-10. ECP Parallel Port Forward Timings

11.11 ECP Parallel Port Backward Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	PD[7:0] valid to nAck asserted	0			nsec
t_2	nAck asserted to nAutoFd asserted	70		170	nsec
t_3	nAutoFd asserted to nAck de-asserted	0			nsec
t_4	nAck de-asserted to nAutoFd de-asserted	70		170	nsec
t_5	nAutoFd de-asserted to PD[7:0] changed	0			nsec
t_6	nAutoFd de-asserted to nAck asserted	0			nsec

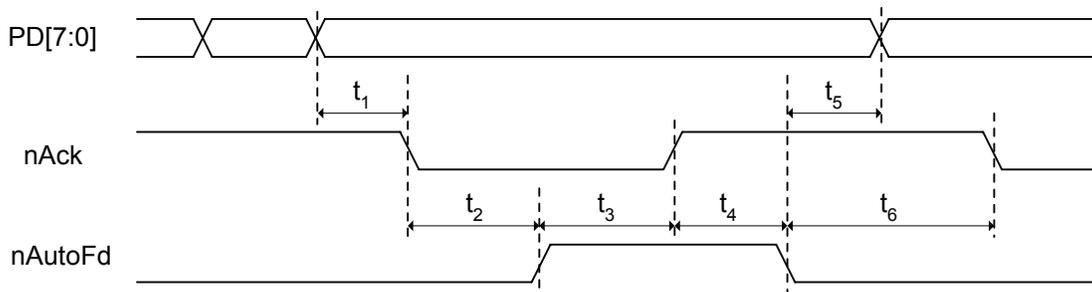


Figure 11-11. ECP Parallel Port Backward Timings

11.12 RSMRST#, PWROK1/2, and ACPI Power Control Signals Timings

Symbol	Parameter	Typ.			Unit
t ₁	RSMRST# de-activates delay from VCCH5V=4V	60			msec
t ₂ *Note1	PWROK1/2 active delay from VCC5V=4V	23h<3:2> =00b	23h<3:2> =01b	23h<3:2> =10b	
		400	15	200	msec
t ₃	Overlap of PSON# and 3VSBSW#	10			msec
t ₄	Delay time of PWROK1/2 and 3VSBSW#	2			msec

Note: PWROK1/2 are set high under the condition of VCC power-level-detect AND RESETCON# AND SUSB# AND ATXPG.

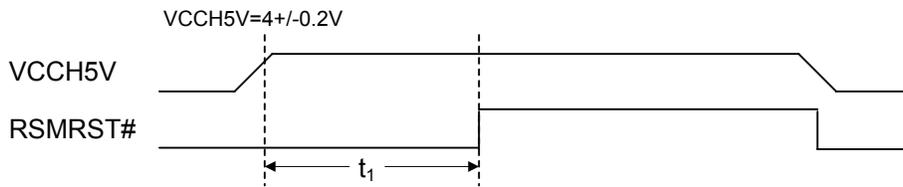


Figure 11-12. RSMRST# Timings

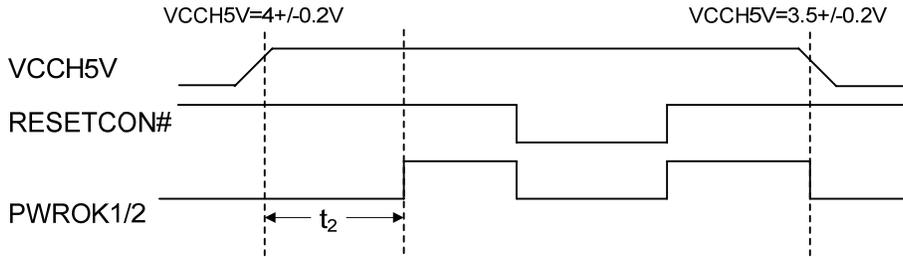


Figure 11-13. PWROK1/2 Timings

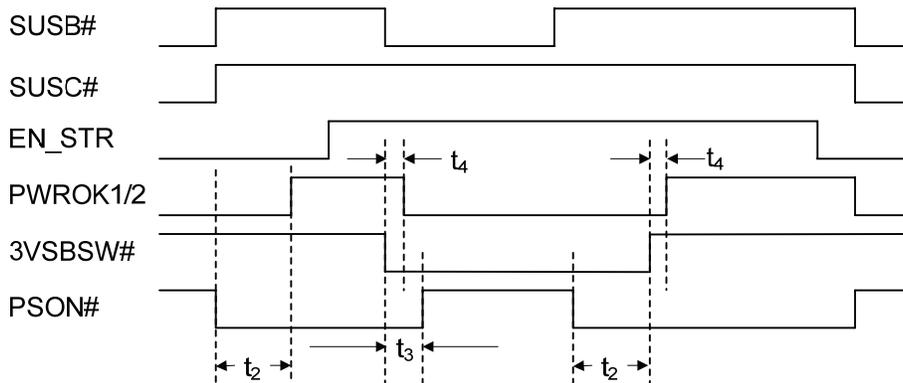


Figure 11-14. ACPI Power signals Timings

11.13 AMD CPU Power Sequence Signals Timings

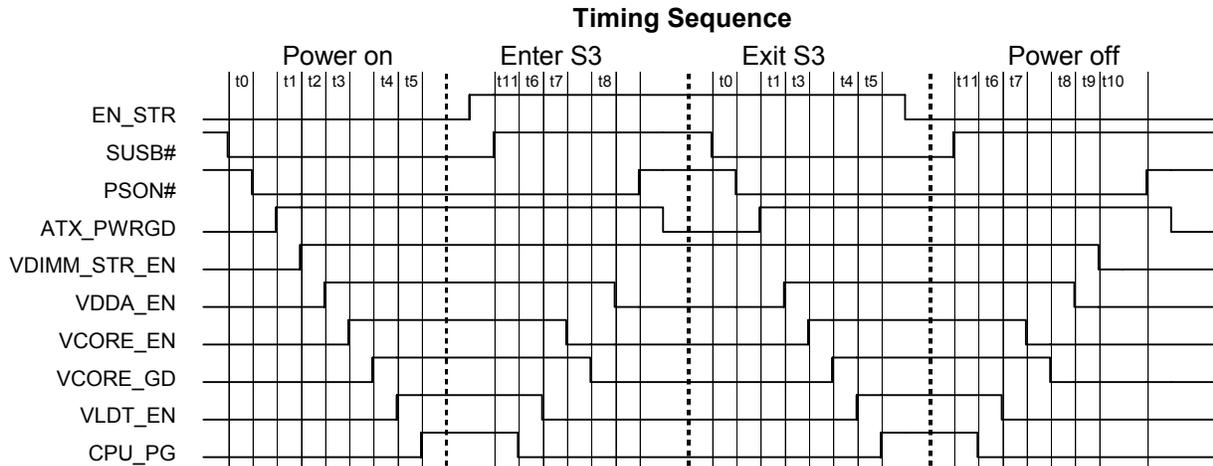


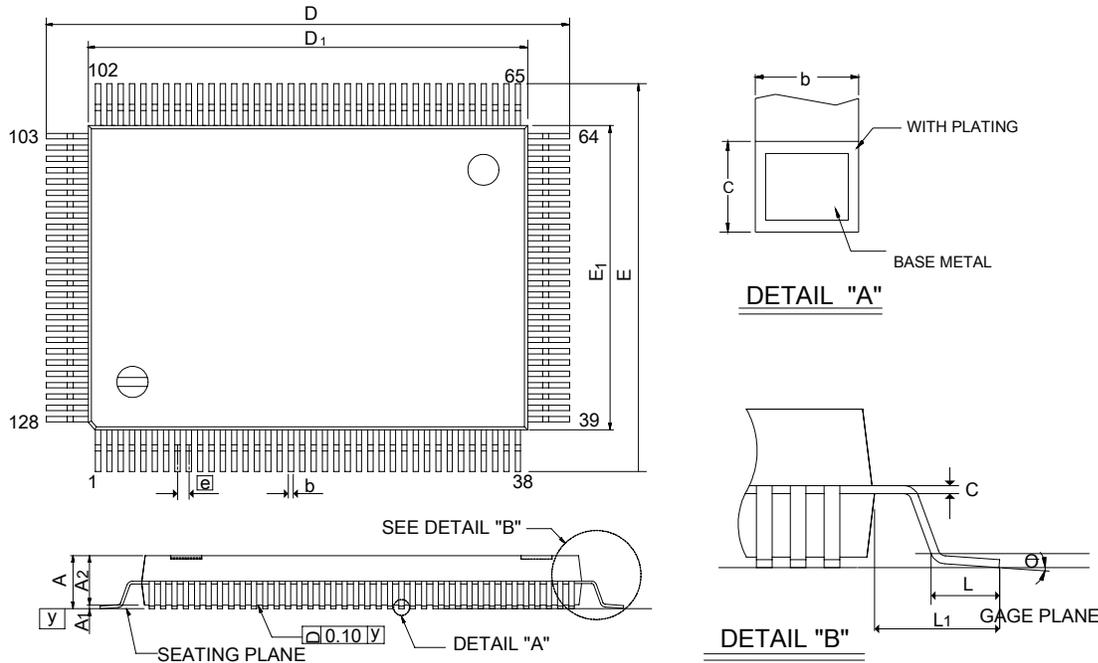
Table 11-1. Power Sequence AC Timing Parameter

Item	Max	Typ	Min	Description
t0		1us	0	The falling edge of SUSB# to the assertion of PSON#.
t1		50us		The rising edge of ATX_PWRGD to the assertion of VDIMM_STR_EN.
t2	2ms + t_vdimm_g d		2ms	The assertion of VDIMM_STR_EN to the assertion of VDDA_EN. The t_vdimm_gd is the rise time of the VDIMM_STR_EN voltage from 0V to 1.62V.
t3	2ms + t_vdda_gd		2ms	The assertion of VDDA_EN to the assertion of VCORE_EN. The t_vdda_gd is the rise time of the VDDA voltage from 0V to 2.25V.
t4		50us		The rising edge of VCORE_GD to the assertion of VLDT_EN.
t5	2ms + t_vldt_gd		2ms	The assertion of VLDT_EN to the assertion of CPU_PWRGD. The t_vldt_gd is the rise time of the VLDT voltage from 0V to 1.0V.
t6		50us		The de-assertion of CPU_PG to the de-assertion of VLDT_EN.
t7		10ms		The de-assertion of VLDT_EN to the de-assertion of VCORE_EN.
t8		150ms		The falling edge of VCORE_GD to the de-assertion of VDDA_EN.
t9		10ms		The de-assertion of VDDA_EN to the de-assertion of VDIMM_STR_EN or PSON#.
t10		50ms		The de-assertion of VDIMM_STR_EN to the de-assertion of PSON#.
t11		50us		The rising edge of SUSB# to the de-assertion of CPU_PG.

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12. Package Information
QFP 128L Outline Dimensions

unit: inches/mm



Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	0.134	-	-	3.40
A ₁	0.010	-	-	0.25	-	-
A ₂	0.107	0.112	0.117	2.73	2.85	2.97
b	0.007	0.009	0.011	0.17	0.22	0.27
c	0.004	-	0.008	0.09	-	0.20
D	0.906	0.913	0.921	23.00	23.20	23.40
D ₁	0.783	0.787	0.791	19.90	20.00	20.10
E	0.669	0.677	0.685	17.00	17.20	17.40
E ₁	0.547	0.551	0.555	13.90	14.00	14.10
e	0.020 BSC			0.5 BSC		
L	0.029	0.035	0.041	0.73	0.88	1.03
L ₁	0.063 BSC			1.60 BSC		
y	-	-	0.004	-	-	0.10
θ	0°	-	7°	0°	-	7°

Notes:

1. Dimensions D₁ and E₁ do not include mold protrusion. But mold mismatch is included.
2. Dimensions b does not include dambar protrusion.
3. Controlling dimension: millimeter

DI-QFP128(14*20)v2

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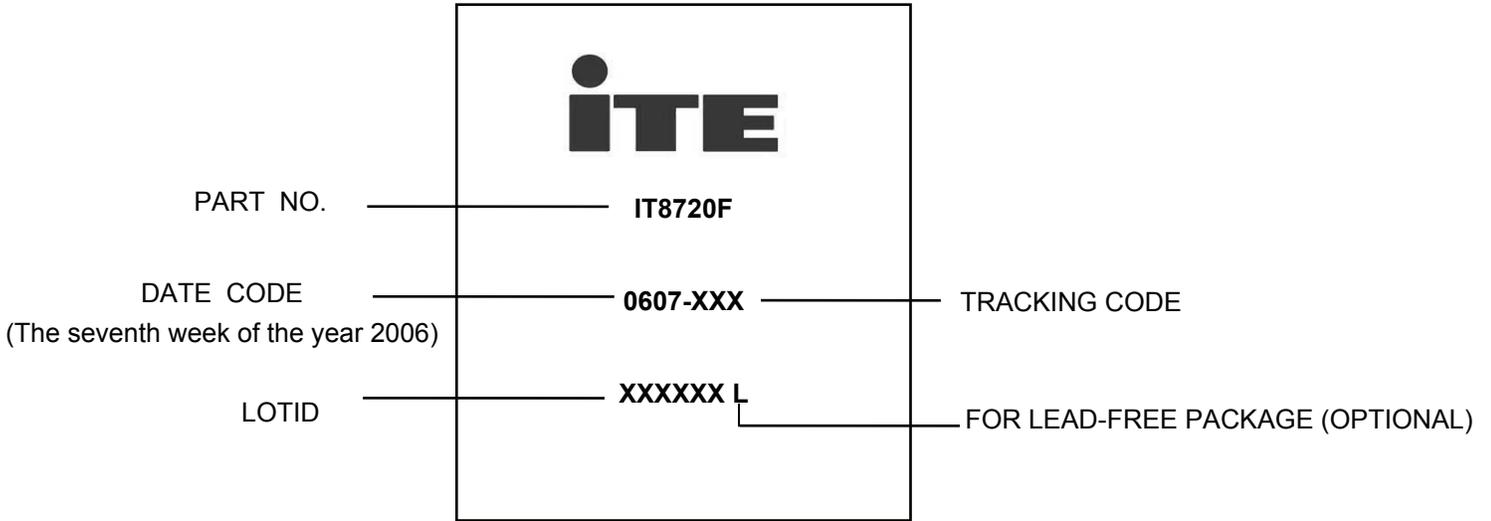
13. Ordering Information

Part No.	Package
IT8720F	128 QFP

ITE also provides RoHS compliant component. Please mark "-L" at the end of the Part No. when the parts ordered are RoHS compliant."

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14. Top Marking Information



0. PARTIES

ITE Tech. Inc. ("Seller") is a company headquartered in Taiwan, Republic of China, and incorporated under laws of Republic of China, Buyer is a company or an entity, purchasing product from ITE Tech. Inc..

1. ACCEPTANCE OF TERMS

BUYER ACCEPTS THESE TERMS (i) BY WRITTEN ACCEPTANCE (BY PURCHASE ORDER OR OTHERWISE), OR (ii) BY FAILURE TO RETURN GOODS DESCRIBED ON THE FACE OF THE PACKING LIST WITHIN FIVE DAYS OF THEIR DELIVERY.

2. DELIVERY

- (a) Delivery will be made Free Carrier (Incoterms), Seller's warehouse, Science-Based Industrial Park, Hsinchu, Taiwan.
- (b) Title to the goods and the entire risk will pass to Buyer upon delivery to carrier.
- (c) Shipments are subject to availability. Seller shall make every reasonable effort to meet the date(s) quoted or acknowledged; and if Seller makes such effort, Seller will not be liable for any delays.

3. TERMS OF PAYMENT

- (a) Terms are as stated on Seller's quotation, or if none are stated, net thirty (30) days. Accounts past due will incur a monthly charge at the rate of one percent (1%) per month (or, if less, the maximum allowed by applicable law) to cover servicing costs.
- (b) Seller reserves the right to change credit terms at any time in its sole discretion.

4. LIMITED WARRANTY

- (a) Seller warrants that the goods sold will be free from defects in material and workmanship and comply with Seller's applicable published specifications for a period of ninety (90) days from the date of Seller's delivery. Within the warranty period and by obtaining a return number from Seller, Buyer may request replacement or repair for defective goods.
- (b) Goods or parts which have been subject to abuse (including without limitation repeated or extended exposure to conditions at or near the limits of applicable absolute ratings) misuse, accident, alteration, neglect, or unauthorized repair or improper application are not covered by any warranty. No warranty is made with respect to custom products or goods produced to Buyer's specifications (unless specifically stated in a writing signed by Seller).
- (c) No warranty is made with respect to goods used in devices intended for use in applications where failure to perform when properly used can reasonably be expected to result in significant injury (including, without limitation, navigation, aviation or nuclear equipment, or for surgical implant or to support or sustain life) and Buyer agrees to indemnify, defend, and hold harmless Seller from all claims, damages and liabilities arising out of any such uses.
- (d) This Paragraph 4 is the only warranty by Seller with respect to goods and may not be modified or amended except in writing signed by an authorized officer of Seller.
- (e) Buyer acknowledges and agrees that it is not relying on any applications, diagrams or circuits contained in any literature, and Buyer will test all parts and applications under extended field and laboratory conditions. Notwithstanding any cross-reference or any statements of compatibility, functionality, interchangeability, and the like, the goods may differ from similar goods from other vendors in performance, function or operation, and in areas not contained in the written specifications, or as to ranges and conditions outside such specifications; and Buyer agrees that there are no warranties and that Seller is not responsible for such things.
- (f) EXCEPT AS PROVIDED ABOVE, SELLER MAKES NO WARRANTIES OR CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY; AND SELLER EXPRESSLY EXCLUDES AND DISCLAIMS ANY WARRANTY OR CONDITION OF MERCHANTABILITY OR FITNESS FOR PARTICULAR PURPOSE OR APPLICATION.

5. LIMITATION OF LIABILITY

- (a) Seller will not be liable for any loss, damage or penalty resulting from causes beyond its reasonable control, including but not limited to delay by others, force majeure, acts of God, or labor conditions. In any such event, the date(s) for Seller's performance will be deemed extended for a period equal to any delay resulting.
- (b) THE LIABILITY OF SELLER ARISING OUT OF THE CONTRACT OR ANY GOODS SOLD WILL BE LIMITED TO REFUND OF THE PURCHASE PRICE OR REPLACEMENT OF PURCHASED GOODS (RETURNED TO SELLER FREIGHT PRE-PAID) OR, WITH SELLER'S PRIOR WRITTEN CONSENT, REPAIR OF PURCHASED GOODS.
- (c) Buyer will not return any goods without first obtaining a customer return order number.
- (d) AS A SEPARATE LIMITATION, IN NO EVENT WILL SELLER BE LIABLE FOR COSTS OF SUBSTITUTE GOODS; FOR ANY SPECIAL, CONSEQUENTIAL, INCIDENTAL OR INDIRECT DAMAGES; OR LOSS OF USE, OPPORTUNITY, MARKET POTENTIAL, AND/OR PROFIT ON ANY THEORY (CONTRACT, TORT, FROM THIRD PARTY CLAIMS OR OTHERWISE). THESE LIMITATIONS SHALL APPLY NOTWITHSTANDING ANY FAILURE OF ESSENTIAL PURPOSE OF ANY REMEDY.
- (e) No action against Seller, whether for breach, indemnification, contribution or otherwise, shall be commenced more than one year after the cause of action has accrued, or more than one year after either the Buyer, user or other person knew or with reasonable diligence should have known of the matter or of any claim of dissatisfaction or defect involved; and no such claim may be brought unless Seller has first been given commercially reasonable notice, a full written explanation of all pertinent details, and a good faith opportunity to resolve the matter.
- (f) BUYER EXPRESSLY AGREES TO THE LIMITATIONS OF THIS PARAGRAPH 5 AND TO THEIR REASONABLENESS.

6. SUBSTITUTIONS AND MODIFICATIONS

Seller may at any time make substitutions for product ordered which do not materially and adversely affect overall performance with the then current specifications in the typical and intended use. Seller reserves the right to halt deliveries and shipments and alter specifications and prices without notice. Buyer shall verify that the literature and information is current before purchasing.

7. CANCELLATION

The purchase contract may not be canceled by Buyer except with written consent by Seller and Buyer's payment of reasonable cancellation charges (including but not be limited to expenses already incurred for labor and material, overhead, commitments made by Seller, and a reasonable profit).

8. INDEMNIFICATION

Seller will, at its own expense, assist Buyer with technical support and information in connection with any claim that any parts as shipped by Seller under the purchase order infringe any valid and enforceable copyright, or trademark, provided however, that Buyer (i) gives immediate written notice to Seller, (ii) permits Seller to participate and to defend if Seller requests to do so, and (iii) gives Seller all needed information, assistance and authority. However, Seller will not be responsible for infringements resulting from anything not entirely manufactured by Seller, or from any combination with products, equipment, or materials not furnished by Seller. Seller will have no liability with respect to intellectual property matters arising out of products made to Buyer's specifications, code, or designs. Except as expressly stated in this Paragraph 8 or in another writing signed by an authorized officer, Seller makes no representations and/or warranties with respect to intellectual and/or industrial property and/or with respect to claims of infringement. Except as to claims Seller agrees in writing to defend, BUYER WILL INDEMNIFY, DEFEND AND HOLD HARMLESS SELLER FROM ALL CLAIMS, COSTS, LOSSES, AND DAMAGES (INCLUDING ATTORNEYS FEES) AGAINST AND/OR ARISING OUT OF GOODS SOLD AND/OR SHIPPED HEREUNDER.

9. NO CONFIDENTIAL INFORMATION

Seller shall have no obligation to hold any information in confidence except as provided in a separate non-disclosure agreement signed by both parties.

10. ENTIRE AGREEMENT

- (a) These terms and conditions are the entire agreement and the only representations and understandings between Seller and Buyer, and no addition, deletion or modification shall be binding on Seller unless expressly agreed to in written and signed by an officer of Seller.
- (b) Buyer is not relying upon any warranty or representation except for those specifically stated here.

11. APPLICABLE LAW

The contract and all performance and disputes arising out of or relating to goods involved will be governed by the laws of R.O.C. (Taiwan, Republic of China), without reference to the U.N. Convention on Contracts for the International Sale of Goods or to conflict of laws principles. Buyer agrees at its sole expense to comply with all applicable laws in connection with the purchase, use or sale of the goods provided hereunder and to indemnify Seller from any failure by Buyer to so comply. Without limiting the foregoing, Buyer certifies that no technical data or direct products thereof will be made available or re-exported, directly or indirectly, to any country to which such export or access is prohibited or restricted under R.O.C. laws or U.S. laws or regulations, unless prior authorization is obtained from the appropriate officials and agencies of the government as required under R.O.C. or U.S. laws or regulations.

12. JURISDICTION AND VENUE

The courts located in Hsinchu, Taiwan, Republic of China, will have the sole and exclusive jurisdiction and venue over any dispute arising out of or relating to the contract or any sale of goods hereunder. Buyer hereby consents to the jurisdiction of such courts.

13. ATTORNEYS' FEES

Reasonable attorneys' fees and costs will be awarded to the prevailing party in the event of litigation involving and/or relating to the enforcement or interpretation of the contract and/or any goods sold under it.